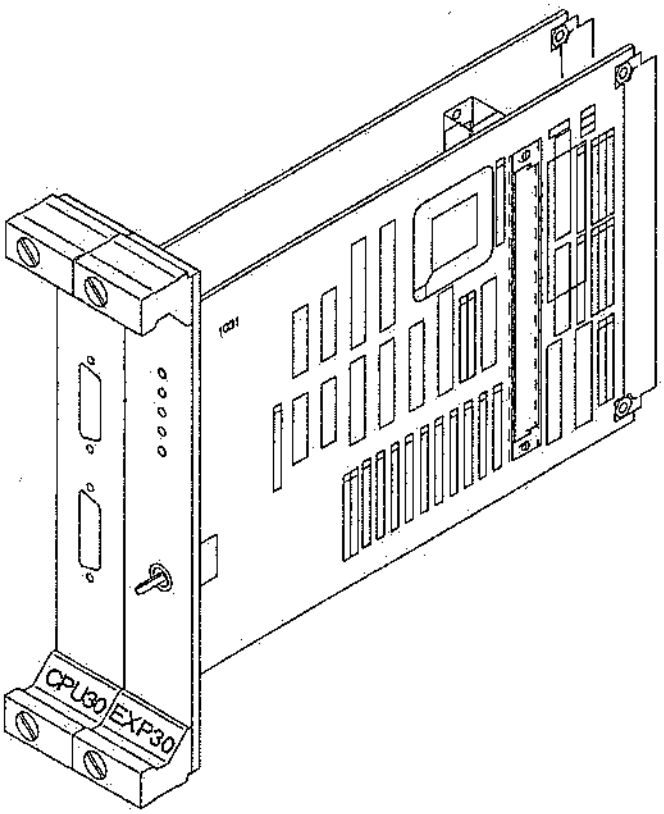
CPU30+EXP30 Kit

Module description

001-7340-xx



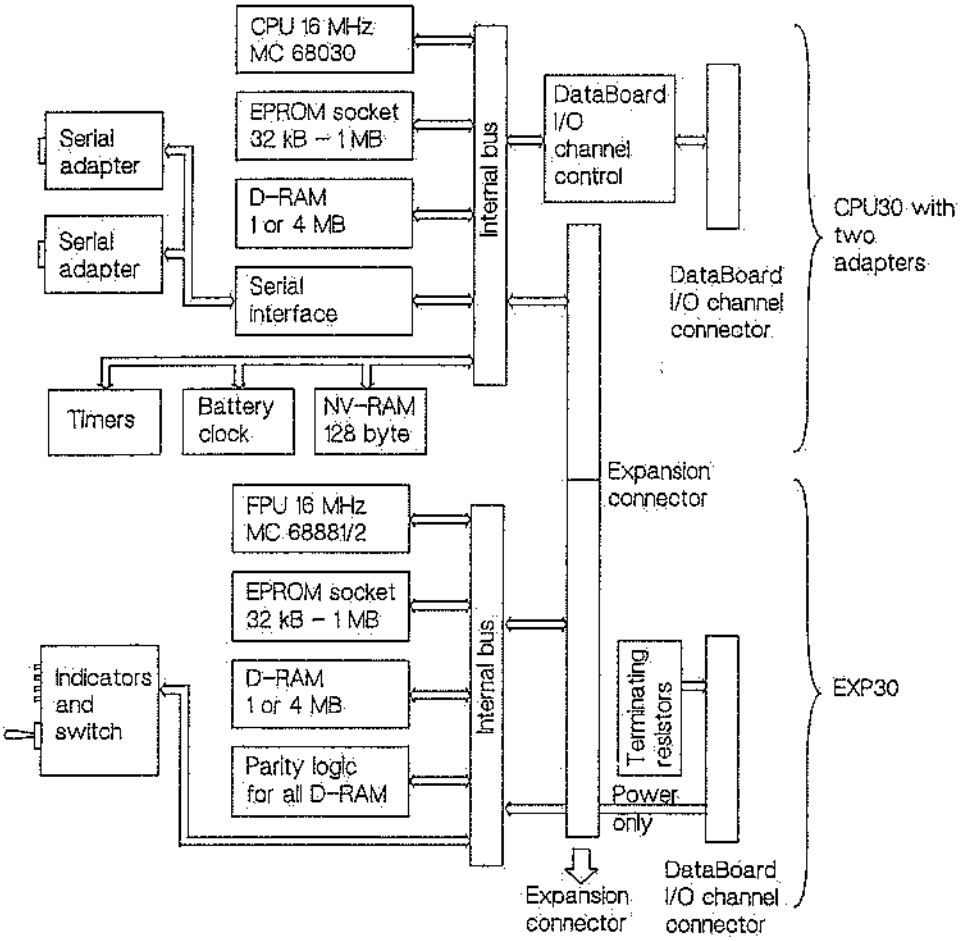
DIAB DATA

Diab Data AB, Box 2029, S-183 02 Täby, Sweden, Telefax +46 8 792 05 61, Phone +46 8 638 94 00

Version A, 90-11-12

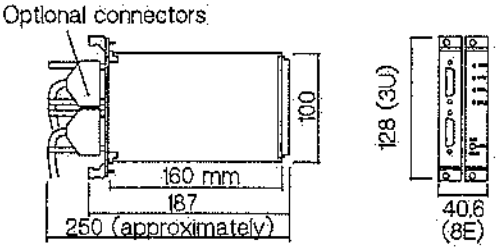
Introduction

The **CPU30+EXP30** kit is a powerful computer module for industrial and technical applications. It contains a CPU30 processor module and an EXP30 expansion module. The start-up program in a boot PROM on CPU30 loads and starts the program from an optional disk structured module.



Technical data

Processor module	CPU30.
Boot PROM	Mounted on the CPU30.
Expansion module	EXP30.
Size:	Two single height Eurocards, mounted together.

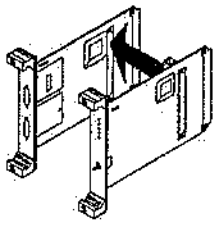


For details, see the appended descriptions.

Configuration

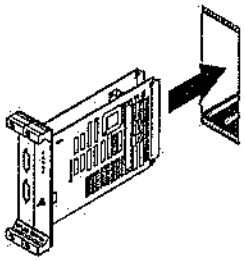
ESD protection is required, e g a wrist band connected to the computer chassis.

Configure each module as described in the enclosed descriptions. DataBoard I/O channel terminations are only mounted on the EXP30.



Mount the expansion board to the expansion connector on the processor module.

Installation



Turn off the power and insert the card stack in a DataBoard rack according to the rack description. Secure the modules to the rack with the four outer screws on the front.

Connectors, indicators and switches

See the appended descriptions for details.

References

DataBoard I/O channel specification.

Version information

Document:
A First version

User documentation page

Project: _____ Date: _____

_____

Please use the User Documentation Pages in the appended descriptions.

CPU30+EXP30 Kit module description

001-7340-xx
Version A

Please give us your opinion on our documentation. Either tell us on this page or make a copy of the page concerned. Staple it to this page and mail it to us.

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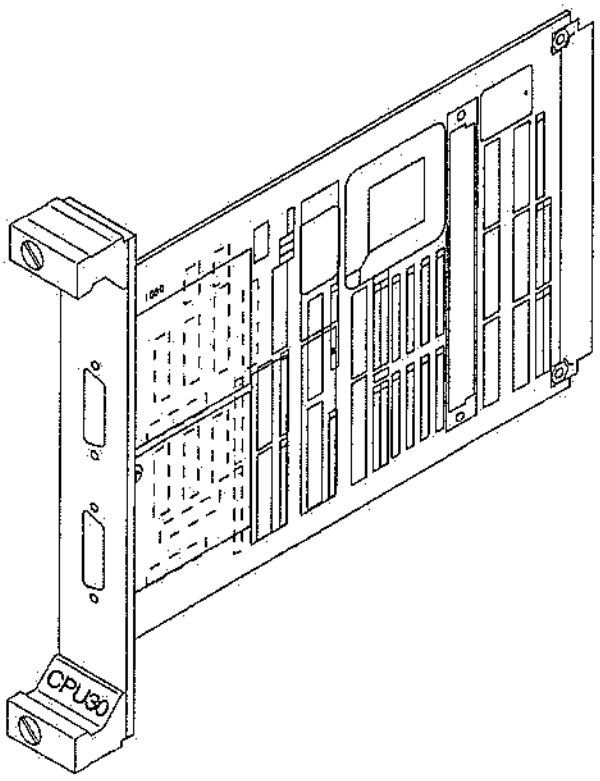
DIAB DATA

MC68030 Processor board

Module description

002-1030-xx



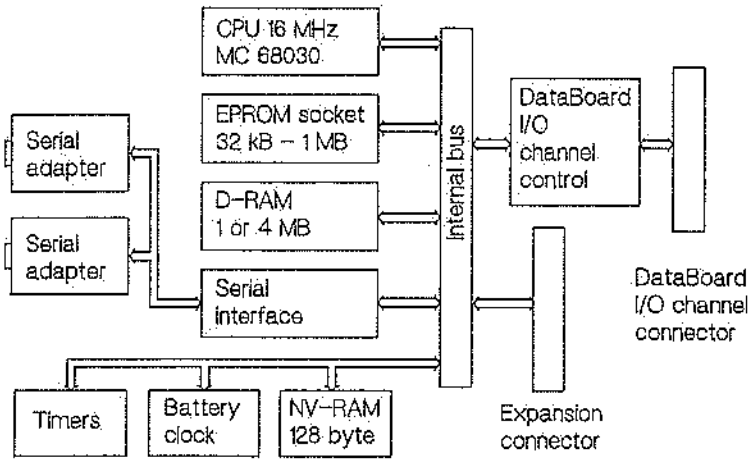
DIAB DATA

Diab Data AB, Box 2029, S-183 02 Täby, Sweden, Telefax +46 8 792 05 61, Phone +46 8 638 94 00

Version A, 90-11-12

Introduction

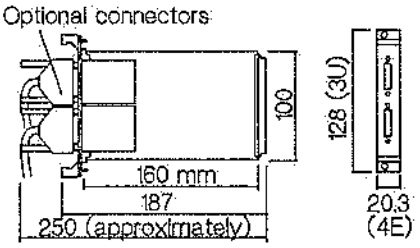
The **CPU30** module is a powerful single board computer for industrial and technical applications. It is well suited for multitask and real time applications. Using different I/O-modules it is used in a large variety of areas, such as data acquisition, data concentration, control and monitoring. The CPU30 is based on the Motorola MC68030 processor and features two high performance serial channels for versatile communication. Expansion modules are mounted on a connector on the board and I/O modules are accessed through the DataBoard I/O channel.



Technical data

CPU	MC68030 CPU at 16 MHz clock.
RAM memory	1 Mbyte or 4 Mbyte D-RAM, 1 wait state. Cache bursts with 1 wait state per burst. 32-bit data bus.
EPROM size	Socket for 32kbyte - 1 Mbyte EPROM.
EPROM type	27C256 - 27C8192 ByteWyde CMOS EPROM in 32- or 28-pin DIP packet. Max 200 ns access time
NV-RAM	NMC9346N, 128 byte, max 10.000 erase/write operations.
Time-of-day clock	Philips PCF8583. Including 240 bytes RAM. 1.2V NiCd battery, providing a minimum of 6 months backup. Charged by the system power.
Serial interface	SCC (Z85C30) with 2 full duplex serial channels, 8.00 MHz clock. Asynchronous/synchronous communication. Asynchronous baudrate 300 - 19200 baud.
Serial adapters	As standard delivered with two serial adapters.
Watchdog	System reset after 250 ms unless pushed. Early warning 200 ms.
Interrupt logic	7 levels of internal hardware interrupts. 8 DataBoard interrupt levels. DataBoard NMI* is one of the hardware interrupts.
System control	CIO (Z8536) circuit with 4.00 MHz clock.
Backplane	DataBoard I/O channel.
Expansion	The internal data bus and control lines are available for up to 3 expansion boards, through an expansion connector .

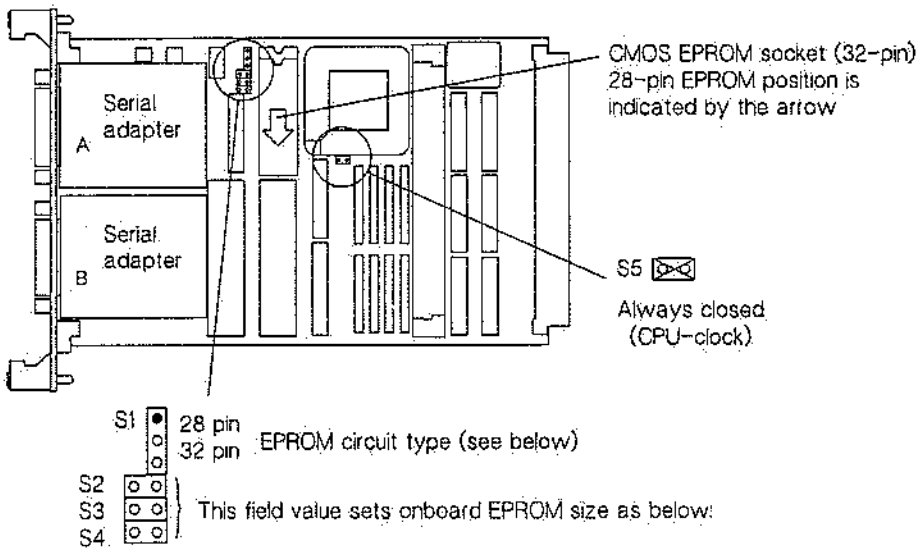
Power	+5V +5%/-2.5%, 3A +12V/-12V used only on the serial adapters. See the adapter description for the requirements.
Environment	0 - 55 °C, 10-80% noncondensing humidity.
Size	Single-height Eurocard.

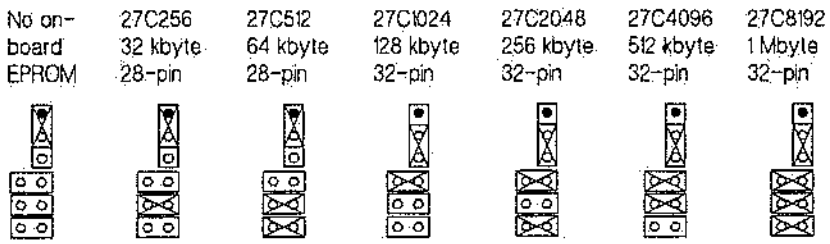


Configuration

ESD protection is required, e g a wrist band connected to the computer chassis.

See the User Configuration Page where the user can enter the actual configuration. Depending on the selected EPROM circuit, set the appropriate jumpers according to the figure below.



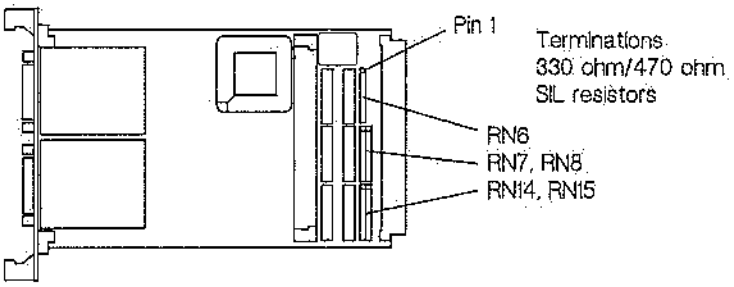


Optional replacement of a serial adapter

See the description for the respective adapter.

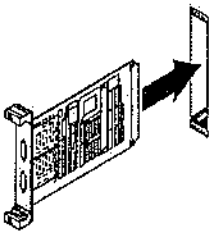
Optional DataBoard I/O channel terminations

If there is no module with terminations connected to the expansion connector and if the used DataBoard backplane does not have terminations, the following termination resistors shall be mounted on CPU30.



Installation

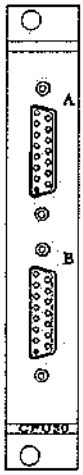
Mount any required expansion boards to the expansion connector on this processor module, before the card stack is inserted in the DataBoard rack.



Turn off the power and insert the module into the CPU slot in a DataBoard rack according to the rack description. Secure the module to the rack with the two outer screws on the front.

Connectors

The module is normally delivered with two serial adapters mounted in the front panel as shown in the figure below. External serial equipments are connected through these connectors. Secure the serial cables using the screws on the connectors.



Serial channel A

Serial channel B

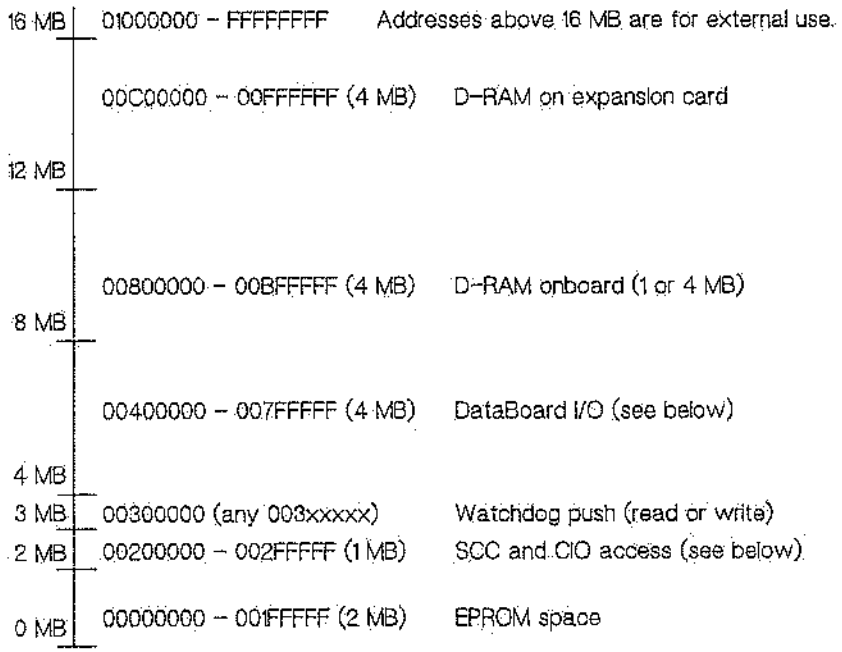
See the User Documentation Page where the user can enter the adapter types mounted and the application units connected. See also the User Documentation Pages for each used adapter, where the user can enter the application signals on the connector pins.

See the **DataBoard I/O channel specification** for details on the backplane connector.

Programming

All resources onboard and support for expansion memory occupy the lowermost 16 Mbyte of the physical address space. Higher addresses are free to use on any optional expansion board, providing the proper acknowledge signals. A bus error occurs 6 microseconds after a non-acknowledged data strobe assertion.

Physical address map



DataBoard I/O channel access

Card select cycles (CS* strobe) on the I/O channel are automatically generated before each data I/O strobe. This module drives the I/O channel lines only during DataBoard I/O cycles. The CPU30 supports the RDY* and WAIT* input lines for high data throughput.

004nnxxx Test mode, returns the Card Select code as data.
Only read cycles are allowed.
005nn0ss Standard DataBoard I/O strobes.
006nnxxx Reads 8-bit CSB* status on the backplane. A bit value '1' indicates that a channel with the corresponding interrupt level is selected.
Only read cycles are allowed.
007nn0ss Enhanced mode DataBoard I/O strobes.
Card select cycles to a previously selected card are suppressed.

nn = Card select code (00 – FF)
ss = Read/write I/O strobe, depending on transfer direction

Read:			Write:		
	INP*	ss = 00		OUT*	ss = 00
	STAT*	ss = 04		C1*	ss = 08
	CPS*	ss = 08		C2*	ss = 0C
				C3*	ss = 10
				C4*	ss = 14

SCC and CIO access

00270000	CIO port C	002B0000	SCC channel B control
00270010	CIO port B	002B0010	SCC channel B data
00270020	CIO port A	002B0020	SCC channel A control
00270030	CIO control	002B0030	SCC channel A data

CIO port usage

The CIO circuit is used for real time clock generation, to detect DataBoard bus interrupts and for communication with the NVRAM and the battery time-of-day clock. In addition it provides general control signals on the expansion connector and two extra timers.

Port A: Connected to the DataBoard interrupt lines.

Bit	Active	Function
PA7	Low	IRQ0* on DataBoard I/O channel (highest priority)
PA6	Low	IRQ1* on DataBoard I/O channel
PA5	Low	IRQ2* on DataBoard I/O channel
PA4	Low	IRQ3* on DataBoard I/O channel
PA3	Low	IRQ4* on DataBoard I/O channel
PA2	Low	IRQ5* on DataBoard I/O channel
PA1	Low	IRQ6* on DataBoard I/O channel
PA0	Low	IRQ7* on DataBoard I/O channel (lowest priority)

Port B: It is used for general system control.

Bit	Active	Function
PB7	High	Asserts and holds the DataBoard RST* signal.
PB6		Only on expansion connector.
PB5		Only on expansion connector.
PB4	Low	Interrupt source to IPL6. Also on the exp. connector.
PB3		Only on expansion connector.
PB2		Only on expansion connector.
PB1		Only on expansion connector.
PB0		Only on expansion connector.

Port C: Used for communication with the NVRAM and the battery clock. In addition PC0 is used as a source for a software initiated interrupt on level IPL1.

Bit	Active	Function
PC3	High	Chip select for the NVRAM only.
PC2	Rising	Serial clock line for battery clock.
PC1	--	Serial data for both NVRAM and battery clock.
PC0	Rising	Bit shift clock for NVRAM (rising edge) and
	Low	also a source of IPL1 interrupt.

Counter/timers:

The C/T 1 is normally used to generate clock interrupts on port B bit 4.

Interrupt system structure

IPL7:	Watch-dog early warning. Autovector, non-maskable.
IPL6:	Generated by driving the CIO port B bit 4 low or from the expansion connector. Autovector.
IPL5:	Interrupt from the SCC. The SCC must supply a vector.
IPL4 :	NMI* interrupt from the DataBoard I/O channel. Autovector.
IPL3:	Interrupt from the CIO. The CIO must provide a vector. Secondary interrupt sources are handled through CIO.
IPL2:	Reserved. Interrupt from the expansion connector. A vector must be provided from the expansion connector.
IPL1:	Generated by driving CIO port C pin 0 low. Autovector.

Power-up sequence
After power-on or system reset, the system will start executing in the EPROM after a delay of 200 ms.

References

DataBoard I/O channel specification.

MC68030 CPU specification (Motorola).

SCC (Z85C30) specification (Zilog).

CIO (Z8536) specification (Zilog).

NMC9346N NV-RAM specification (National Semiconductor).

PCF8583 time-of-day clock specification (Philips).

Version information

Document:
A First version

User documentation page

Project: _____ Date: _____

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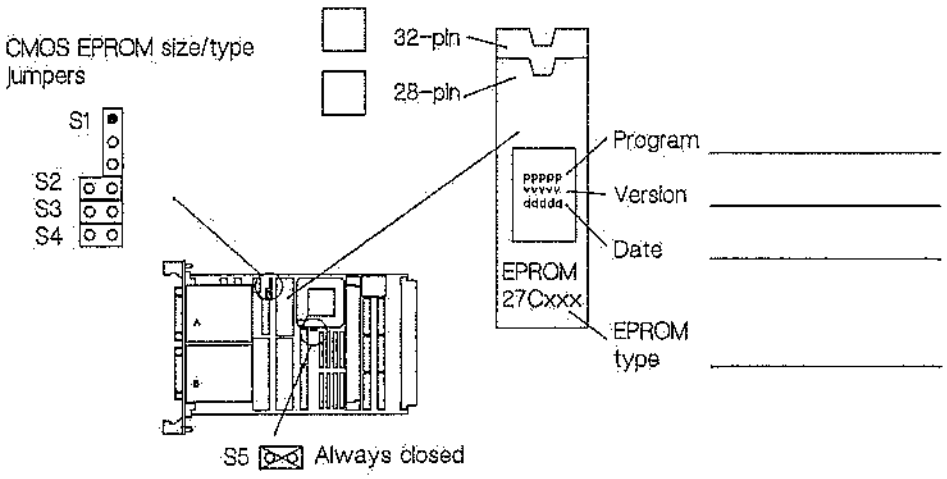
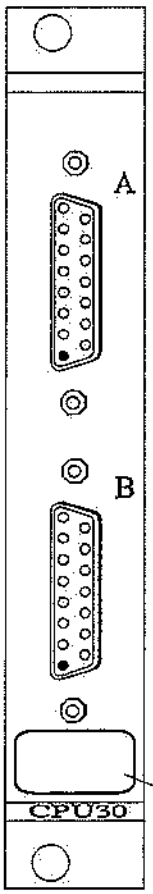
D-RAM memory size: _____





Serial adapter type: _____

Connected to: _____

Serial adapter type: _____

Connected to: _____

CPU30, MC68030 Processor board module description

002-1030-xx
Version A

Please give us your opinion on our documentation. Either tell us on this page or make a copy of the page concerned. Staple it to this page and mail it to us.

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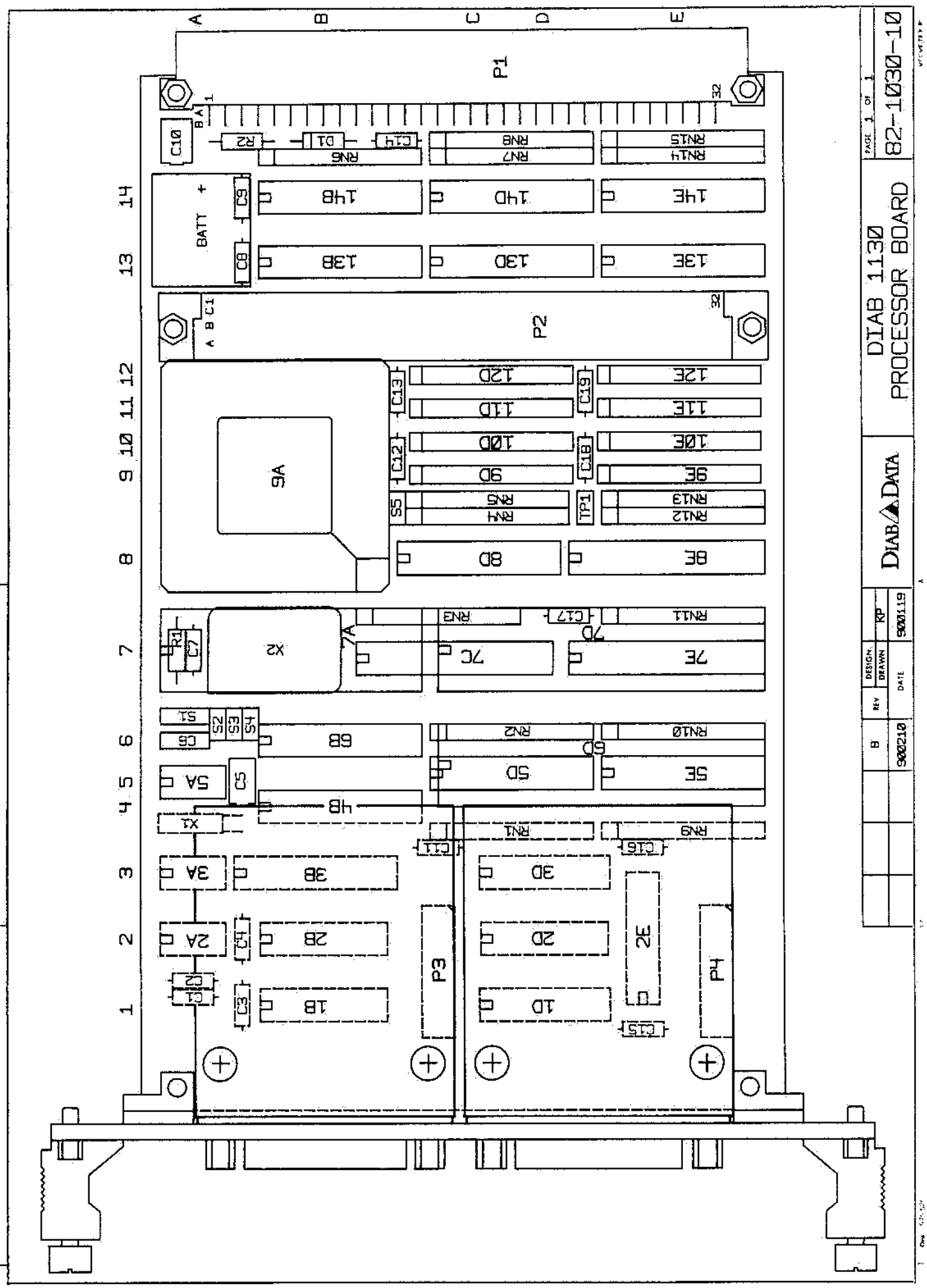
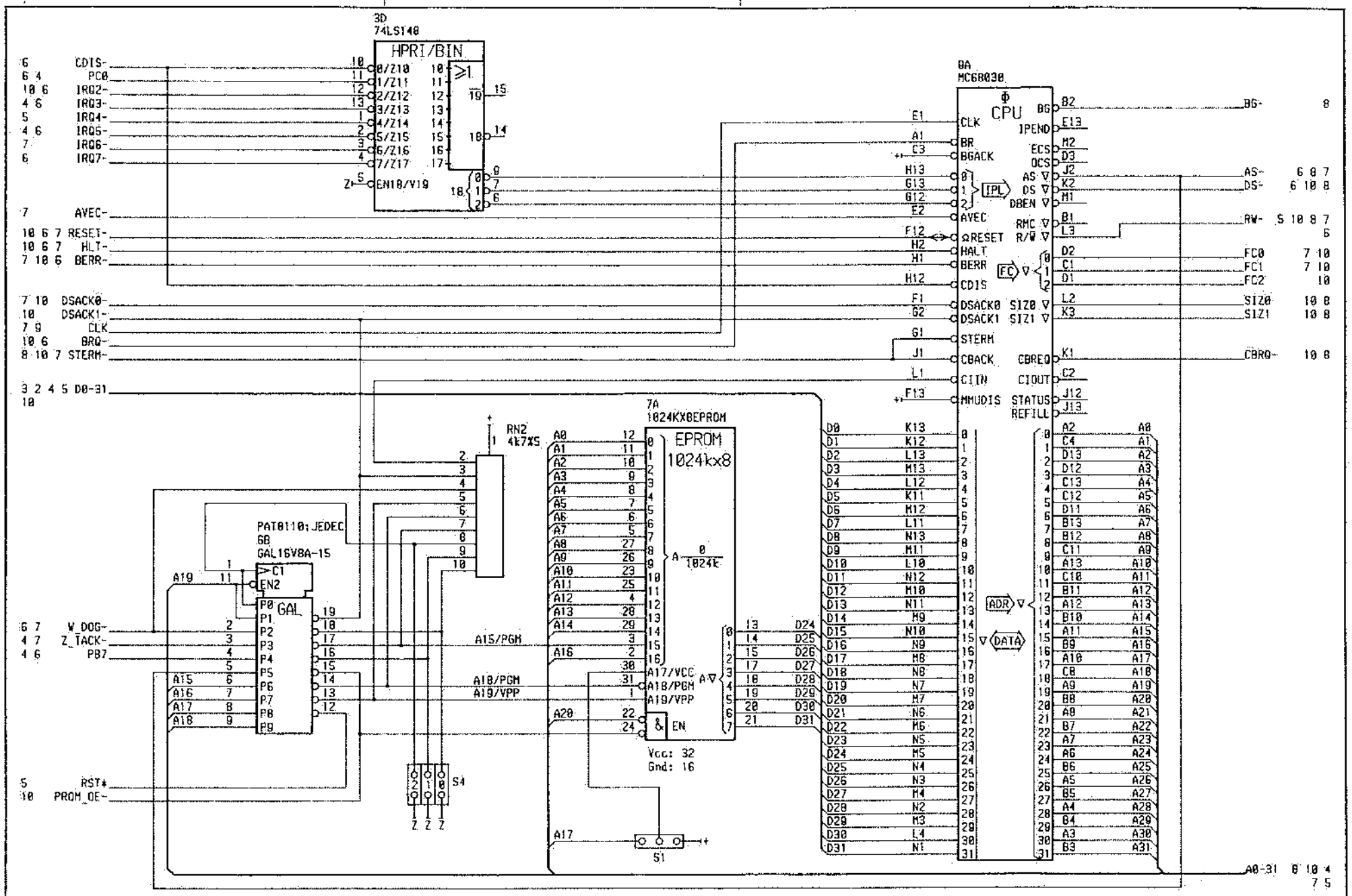
DIAB DATA





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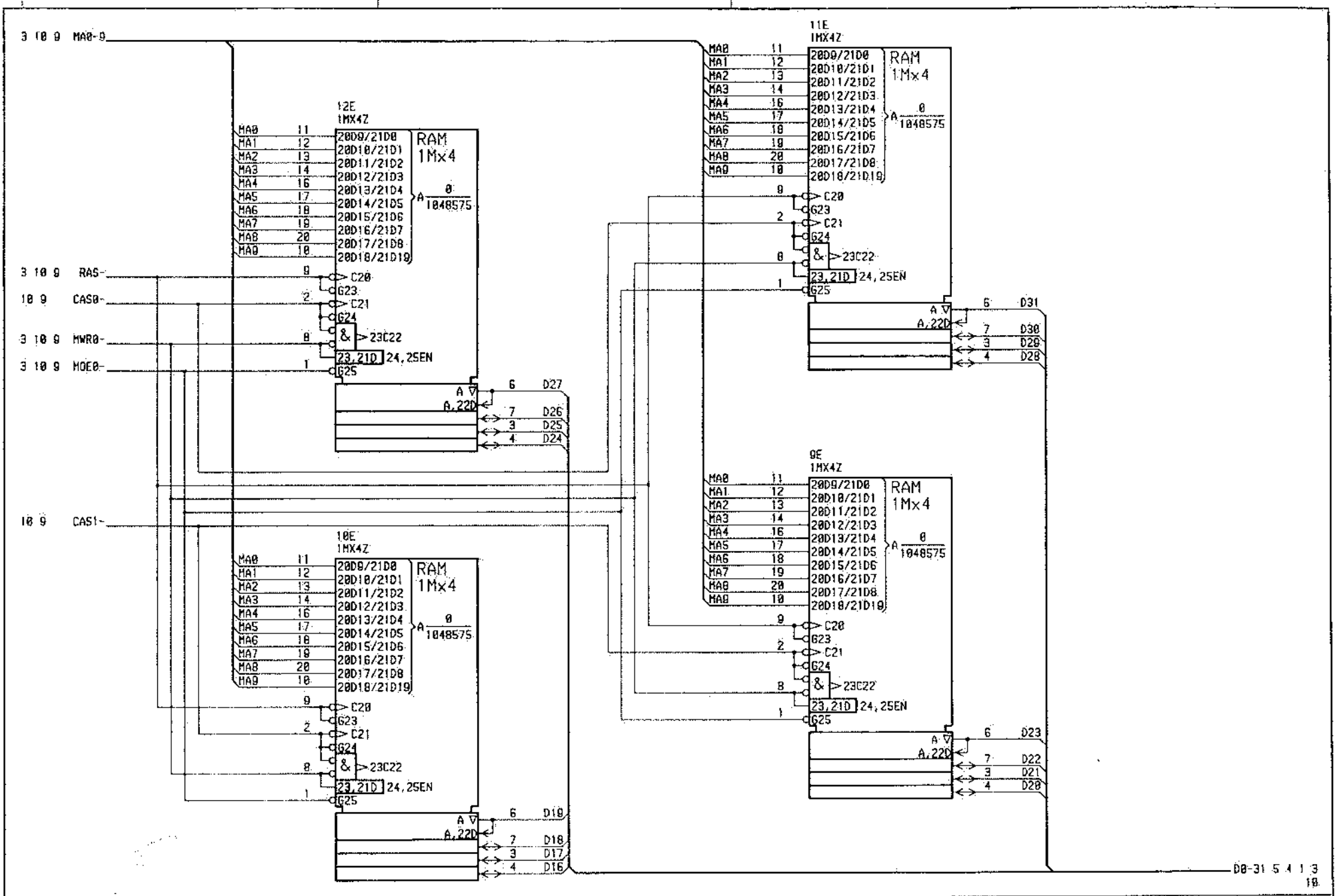
					DATE	900220	

DIAB DATA

CPU and EPROM

PAGE 1 OF 10

81-1030-10



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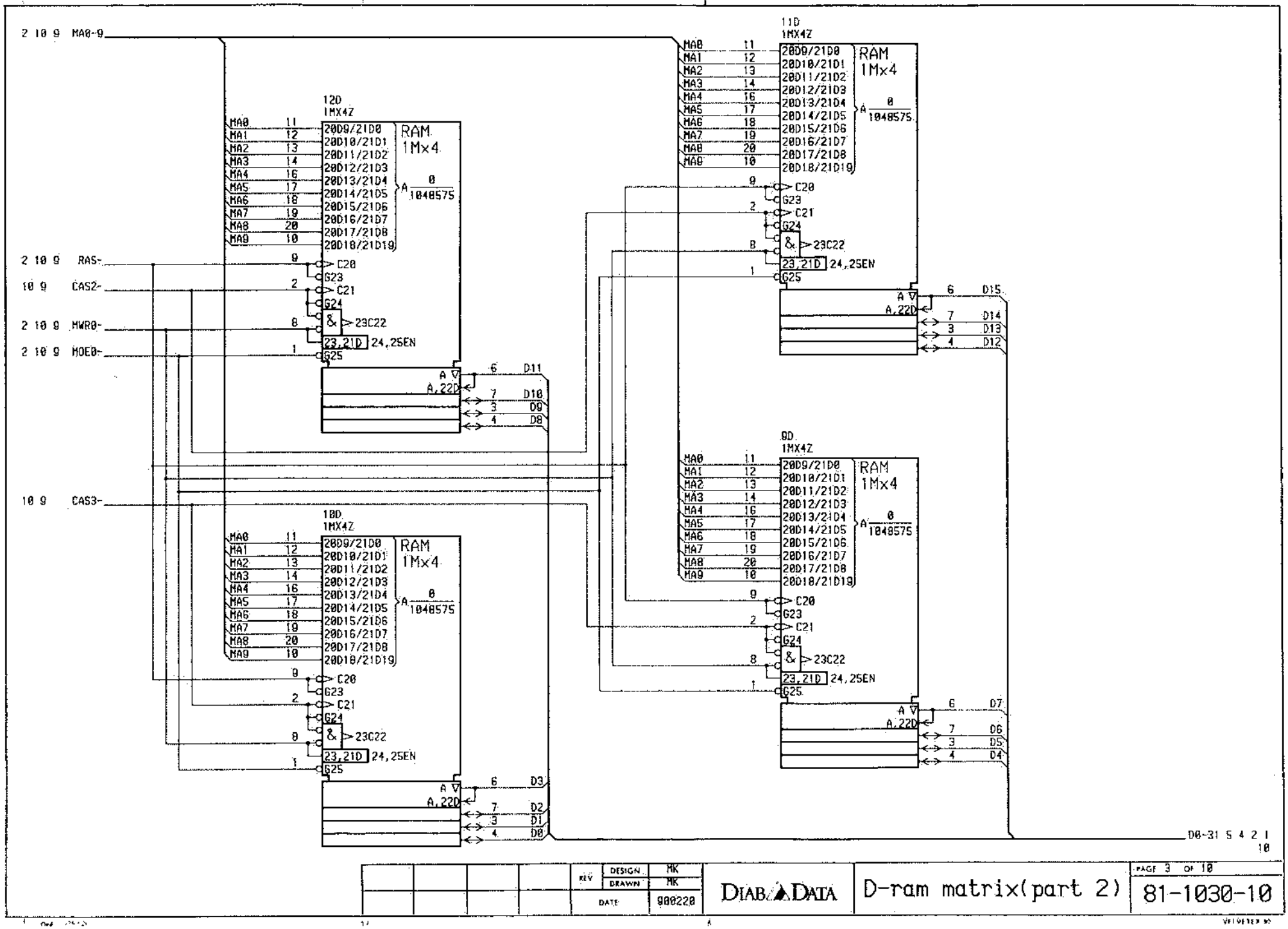
DIAB DATA

D-ram matrix(part 1)

81-1030-10



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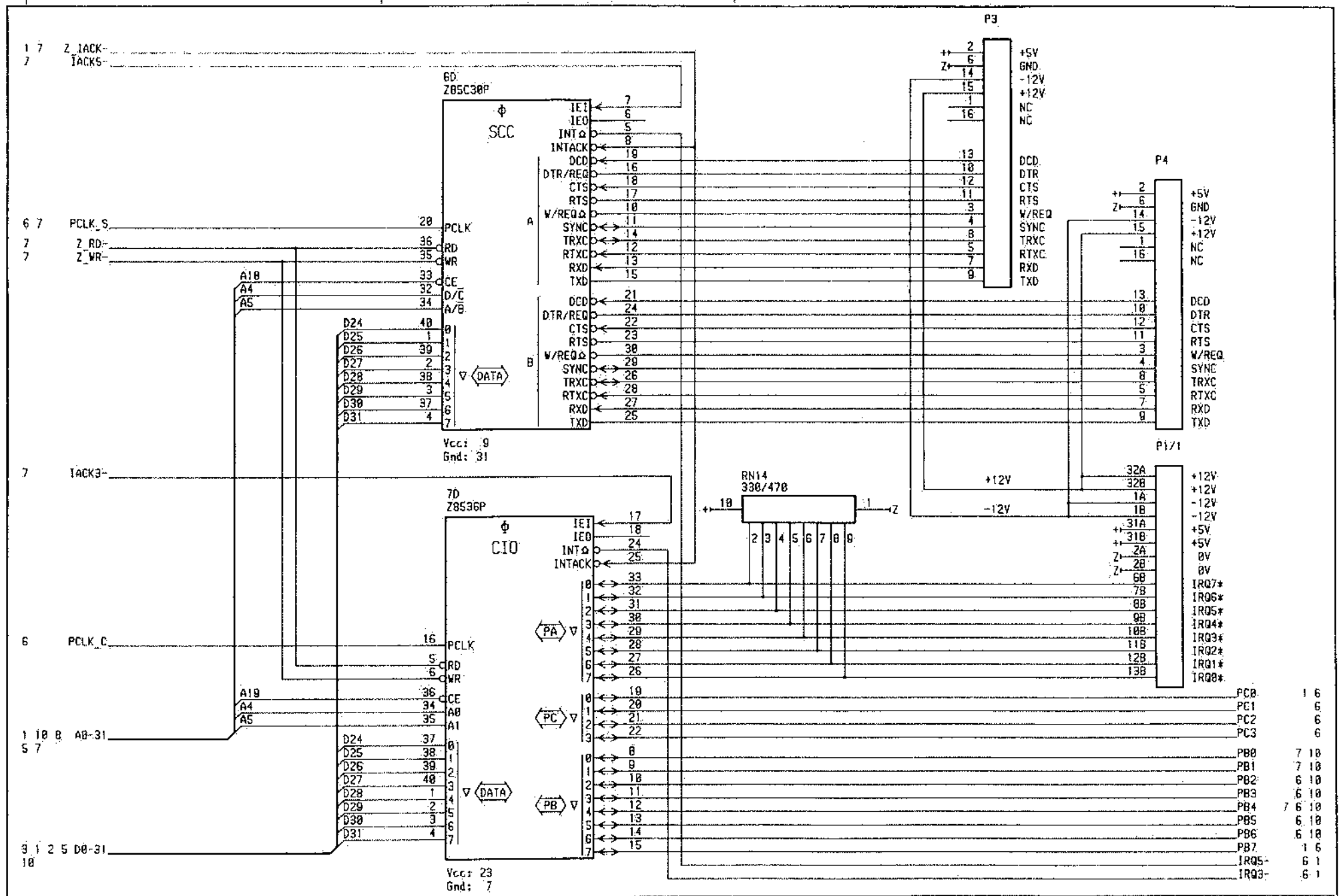
DIAB DATA

D-ram matrix(part 2)

PAGE 3 OF 10

81-1030-10



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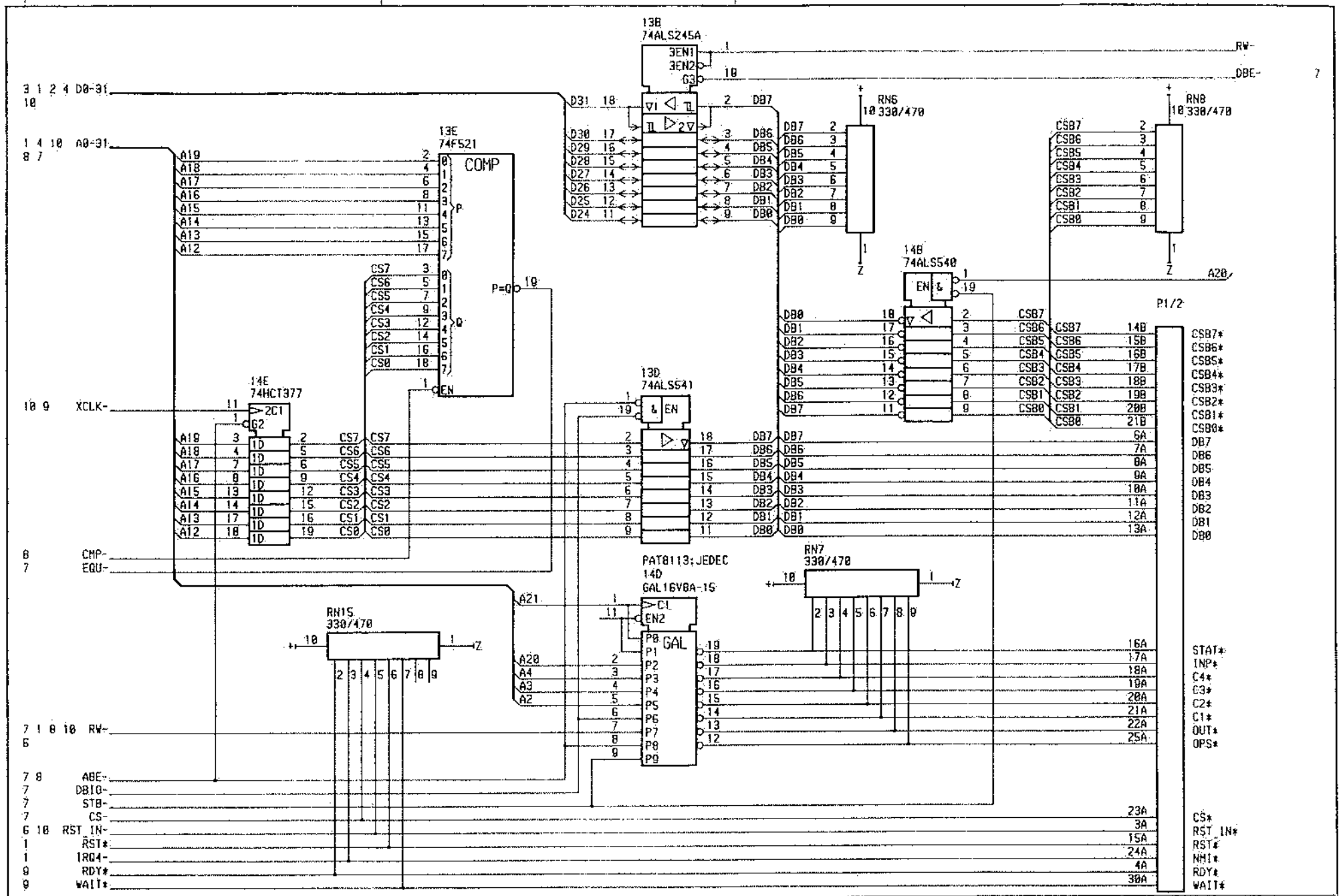
	DATE	900220

DIAB DATA

Port controllers

81-1030-10



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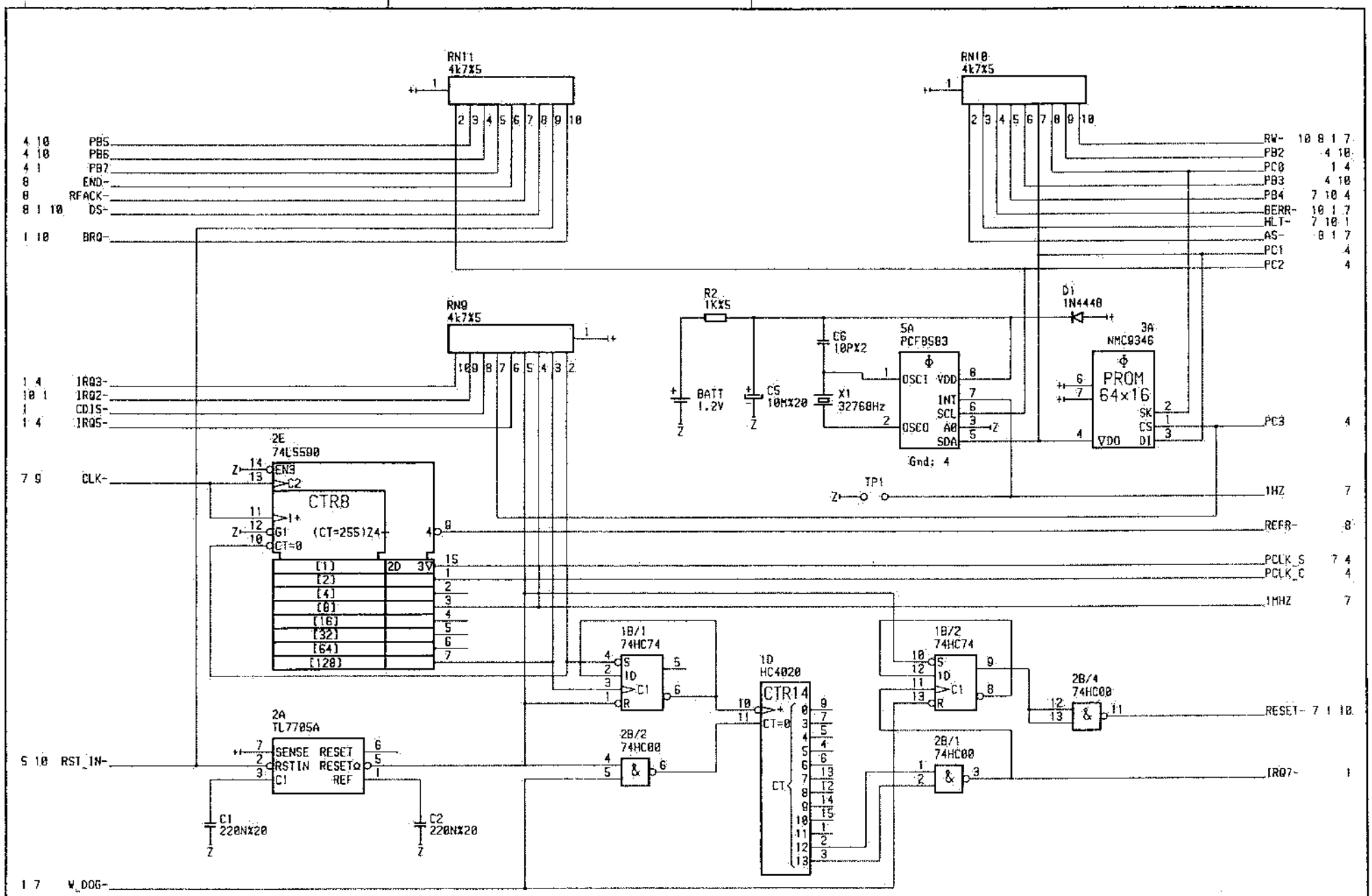
					DRAWN	MK
				DATE	900220	

DIAB/A DATA

DataBoard interface

PAGE 5 OF 10

81-1030-10



				REV	DESIGN	MK	DIAB DATA
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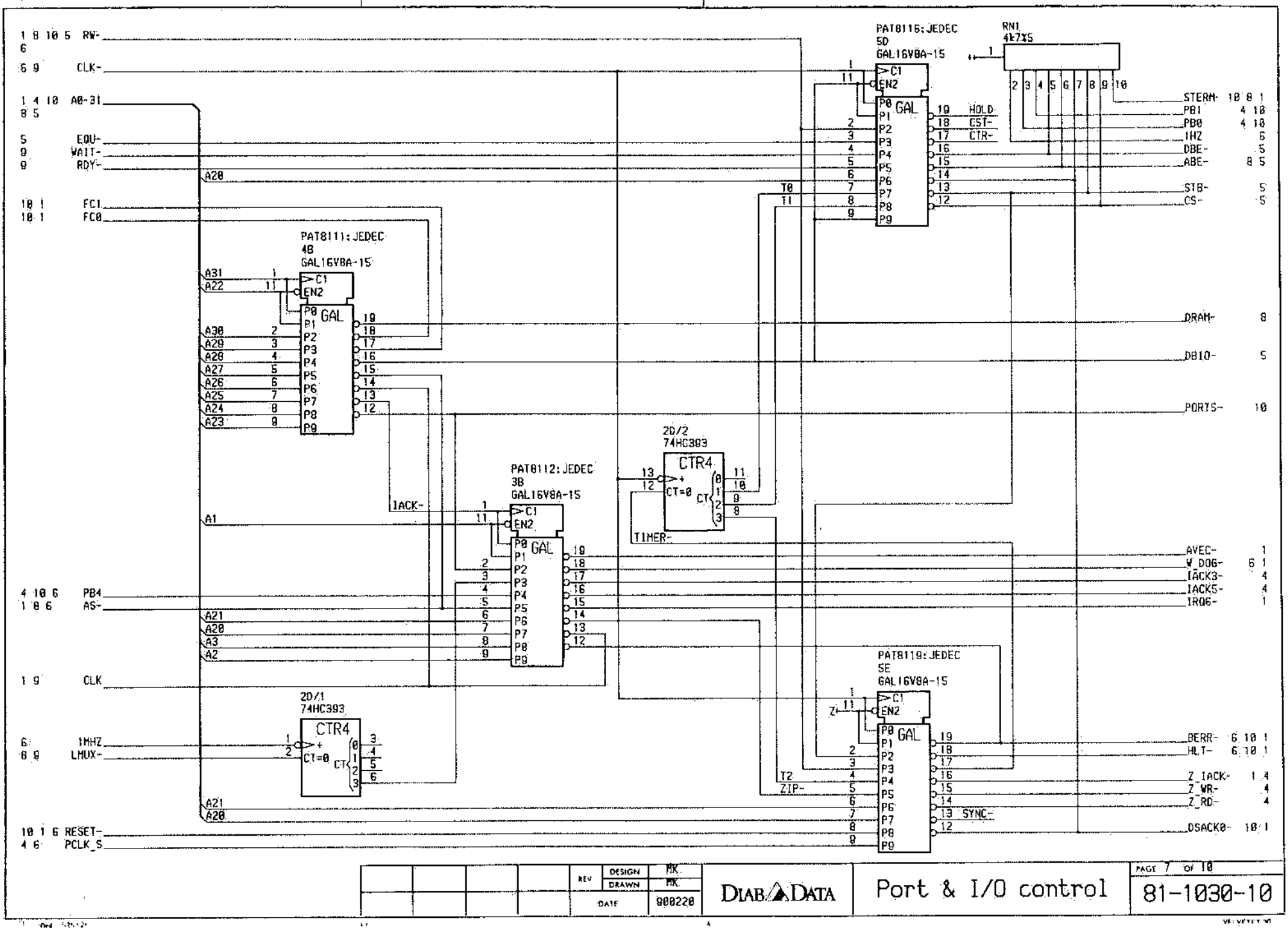
					DATE	000220	81-1030-10



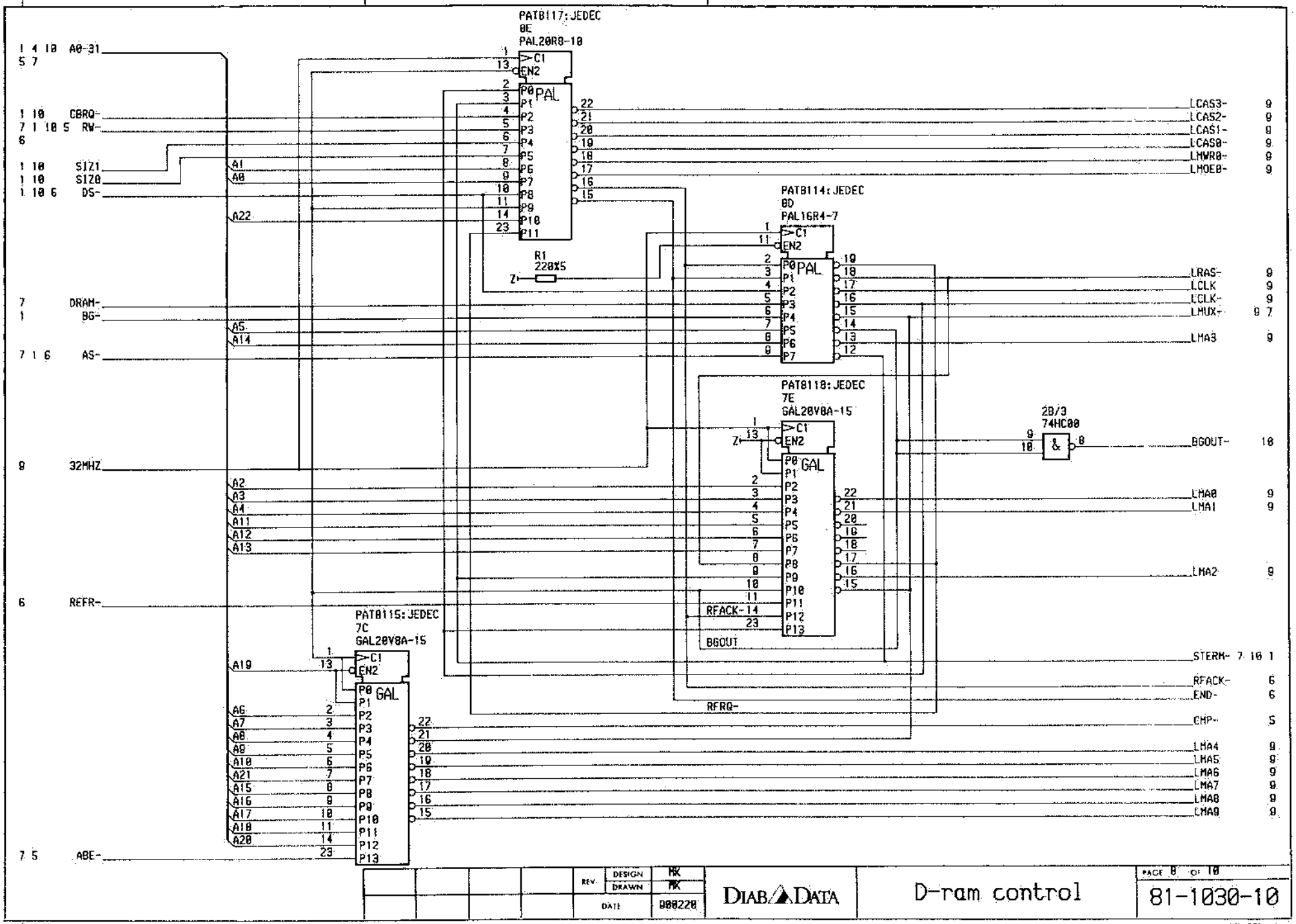
REV	DESIGN	MK
	DRAWN	MK
	DATE	900220

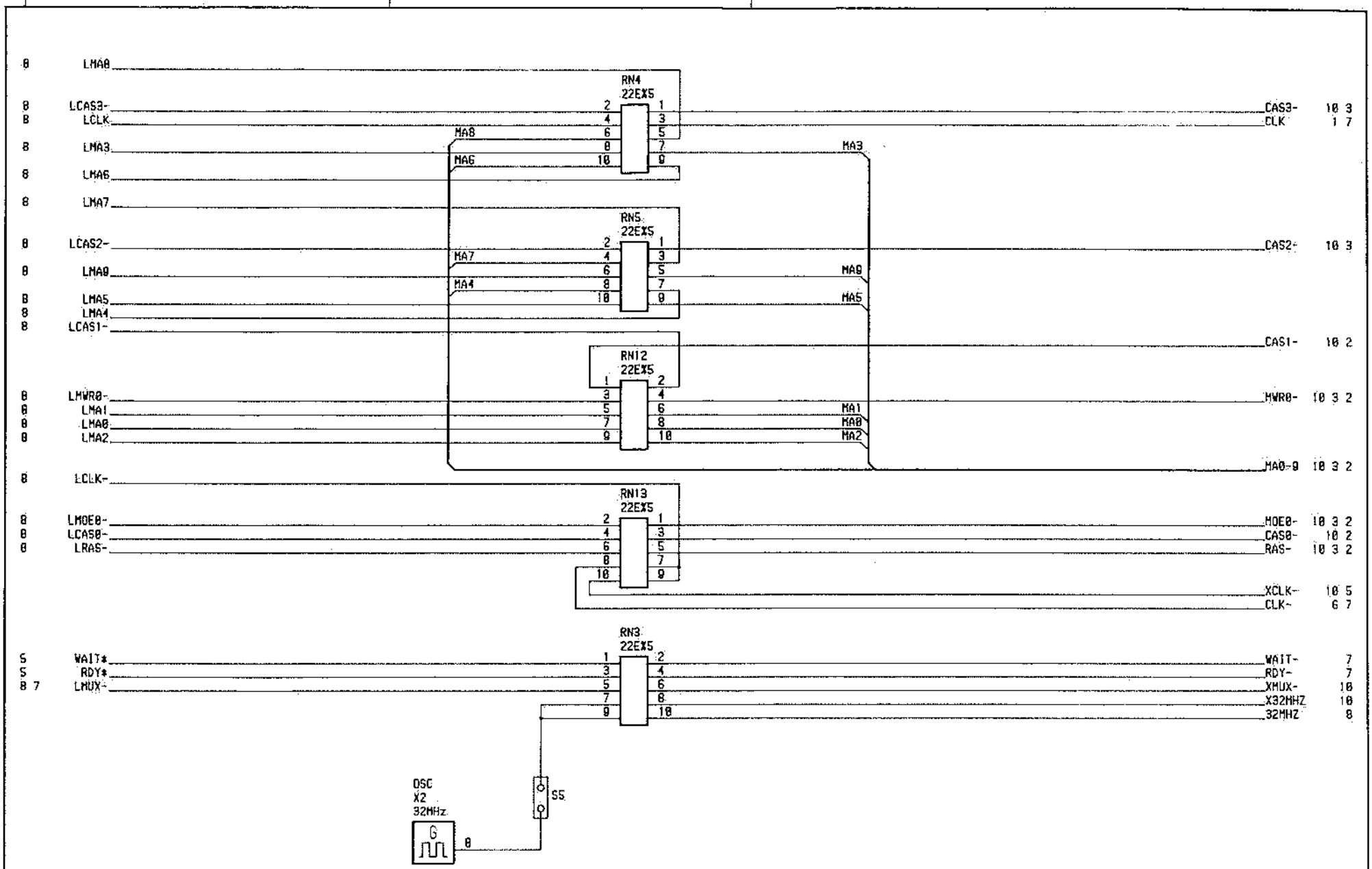
DIAB DATA

Port & I/O control

PAGE 7 OF 10

81-1030-10





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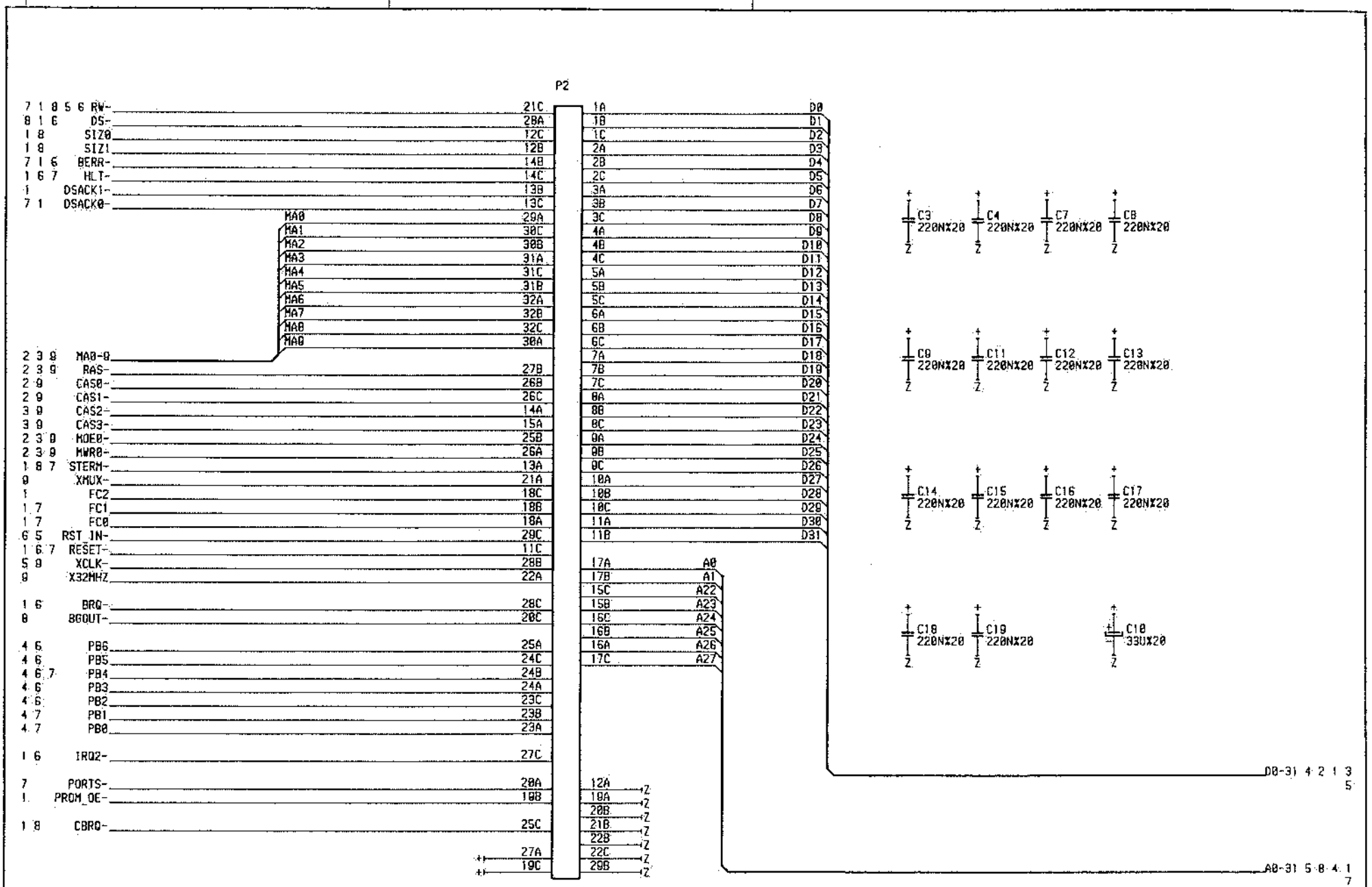
					DRAWN	MK
					DATE	980220

DIAB DATA

Resistor networks

PAGE 9 OF 10

81-1030-10



REV	DESIGN	MK
	DRAWN	MK
	DATE	900220

DIAB DATA

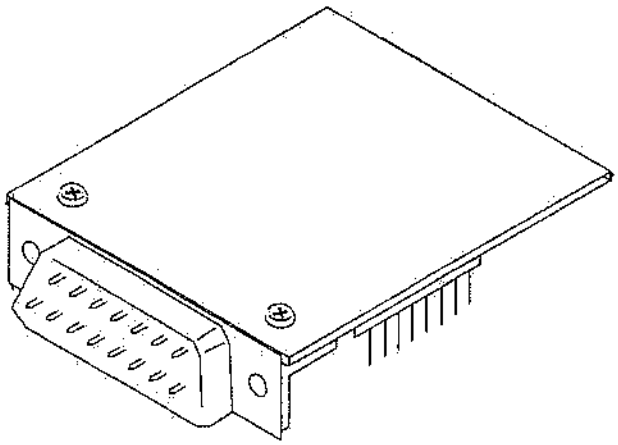
Expansion connector

81-1030-10

V.24 Adapter

Module description

002-5233-xx



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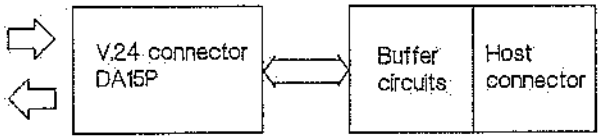
Version B, 90-11-12

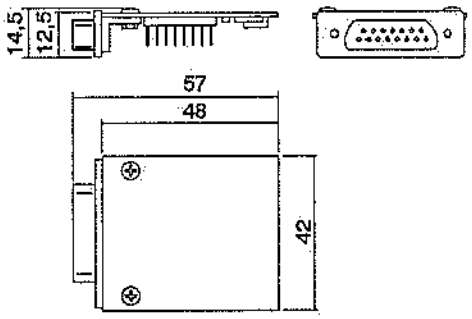
Introduction

The **V24** V.24 adapter module provides buffers and connector for a serial V.24 port, supporting synchronous and asynchronous communication. The adapter is mounted on host modules of different types.



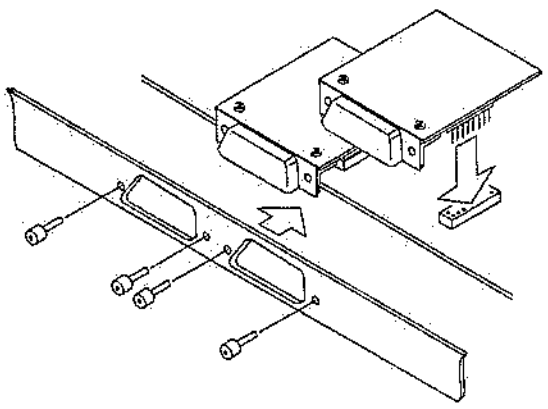
Technical data

I/O	V.24/V.28 level buffer circuits 14C88/14C89 CMOS, limiting the maximum baudrate to 38400 baud.
I/O connector	DA15P D-sub plug connector with screw locks.
Power	+5V +5%/-2.5%, 100 mA +12V +/-10%, 20 mA -12V +/-10%, 20 mA
Environment	0 - 55 °C, 10-80% noncondensing humidity.
Size	See the figure.



Installation

ESD protection is required. A wrist band connected to the computer chassis may for instance be used.



Remove the two screws holding the old adapter to the front panel. A 3/16 inch socket wrench is needed with as small outer diameter as possible.

Either the front panel or the host board is removed to be able to dismount and mount the adapter without damage to the connector pins.

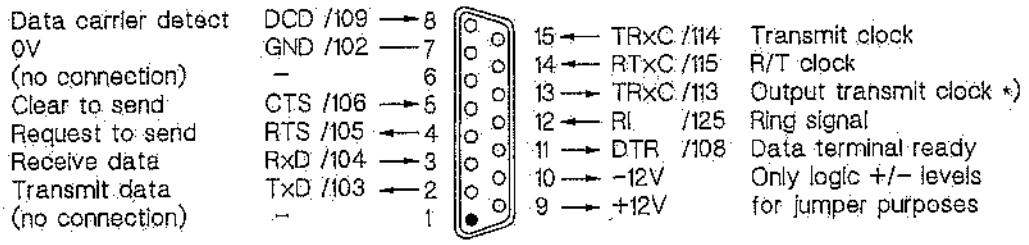
The module is inserted with the component side towards the underlying board on the appropriate 16-pin connector.

Secure the adapter with the two screws to the front panel. Remove any old non-V.24 label from the front panel close to the adapter.

Connectors

The I/O-connector is seen from outside below. See the User Documentation Page where the user can enter the application signals connected.

The actual signal functions depend on the board on which the adapter is mounted.



The RxD input contains a pulldown resistor, to minimize disturbances if a long open-ended cable is connected.

To be able to generate the TRxC clock output (signal 113), the TRxC input (signal 114) must be held at a low level (OFF).

Programming

By temporarily lowering the W/REQ* signal to the adapter, the software on the host can identify the V.24 adapter, as this forces RI (SYNC*) low, which in asynchronous mode sets the sync/hunt bit to one in the SCC. The software must keep the W/REQ* signal high (passive) to allow the RI ring signal input (to the SYNC* pin on the host connector).

References

See the description for the used host module.

Version information

The earlier version (002-5233-10) could source +12V and -12V to external equipments through the I/O connector. These outputs were protected with PTC resistors, which have been replaced by 1 kohm protection resistors from version 002-5233-20.

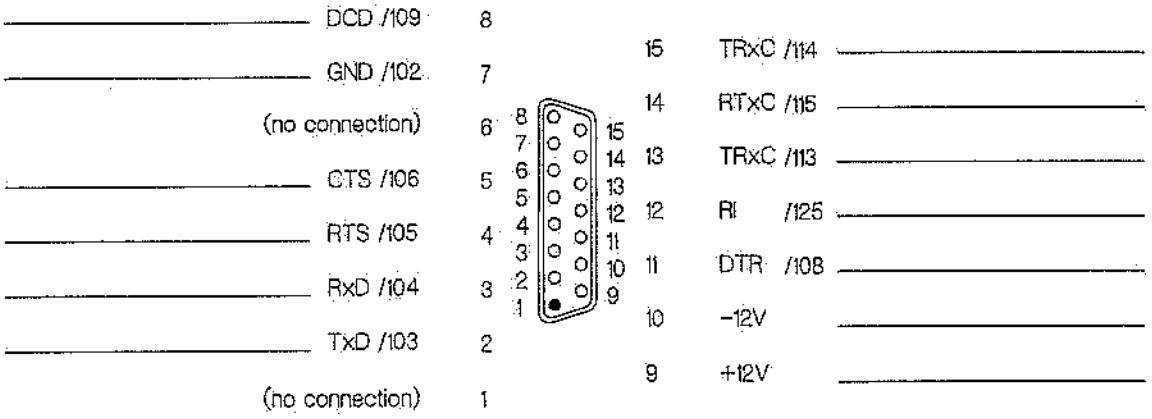
Document:
A First version
B Updated for 002-5233-20

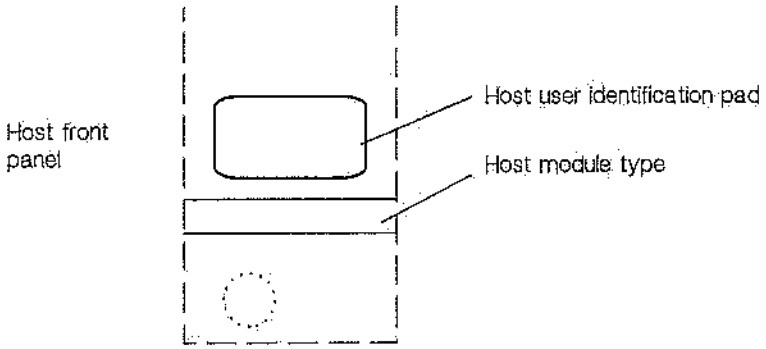
User documentation page

Project: _____ Date: _____

_____

Host channel: _____





V24, V.24 adapter module description

002-5233-xx
Version B

Please give us your opinion on our documentation. Either tell us on this page or make a copy of the page concerned. Staple it to this page and mail it to us.

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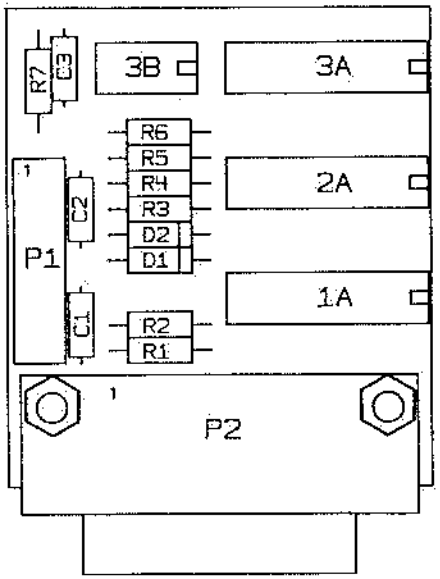
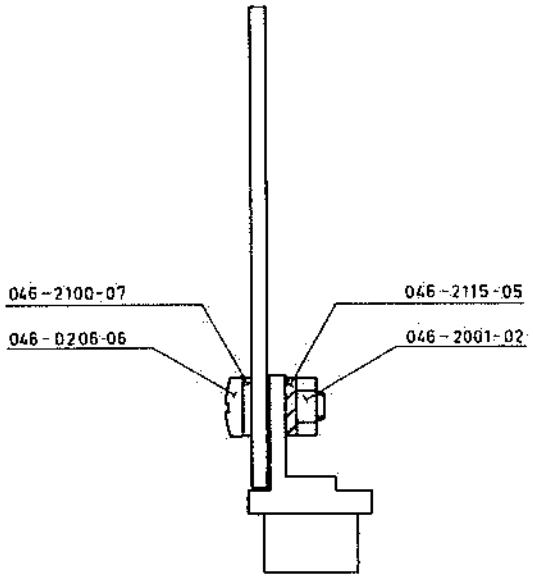
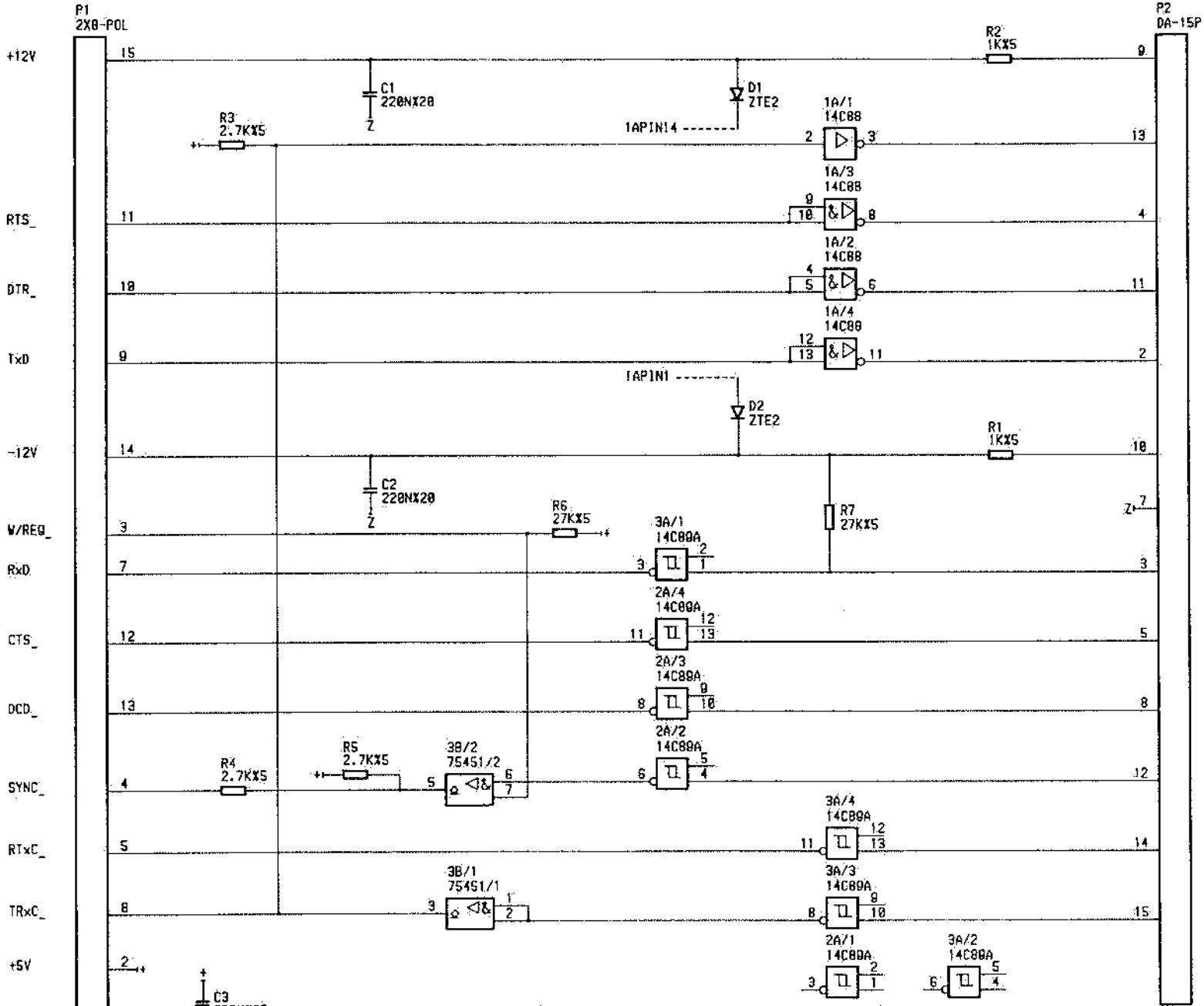
Diab Data AB, Dokumentation, Box 2029, S-183 02 TÄBY, Sweden

DIAB DATA





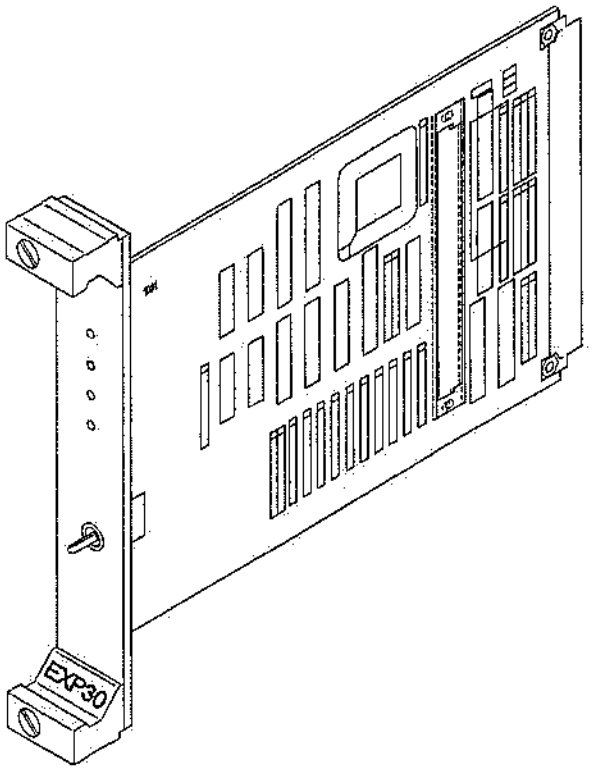
				REV.	DESIGN		DIAB DATA	V.24 ADAPTER	PAGE 1 OF 1
					DRAWN	KP			82-5233-20
				DATE		901009			



Expansion board for CPU30

Module description

002-1031-xx



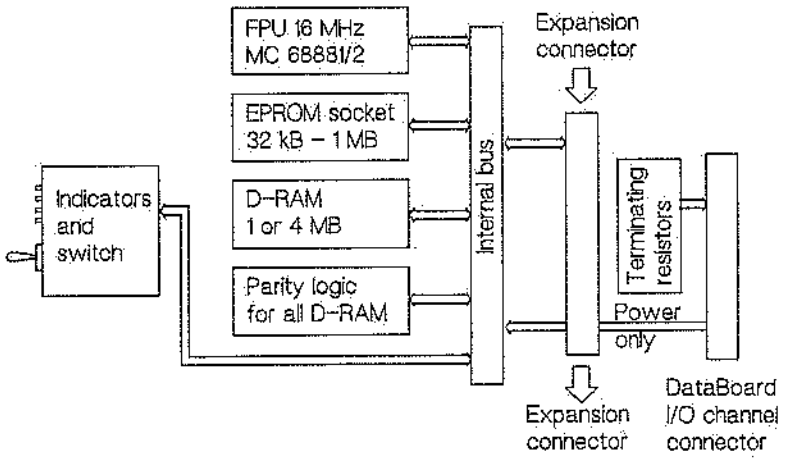
DIAB DATA

Diab Data AB, Box 2029, S-183 02 Täby, Sweden, Telefax +46 8 792 05 61, Phone +46 8 638 94 00

Version A, 90-11-12

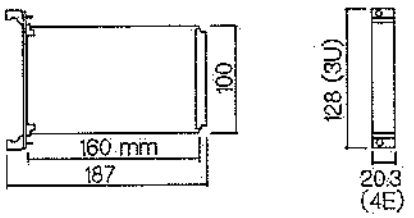
Introduction

The **EXP30** module contains add-on hardware such as memory expansion, memory parity logic and a socket for a floating point coprocessor used by the CPU board. It also provides LED indicators and a switch. These can by choise be used to monitor system activities and to start/stop the system. The EXP30 normally contains termination resistors for the DataBoard I/O channel.



Technical data

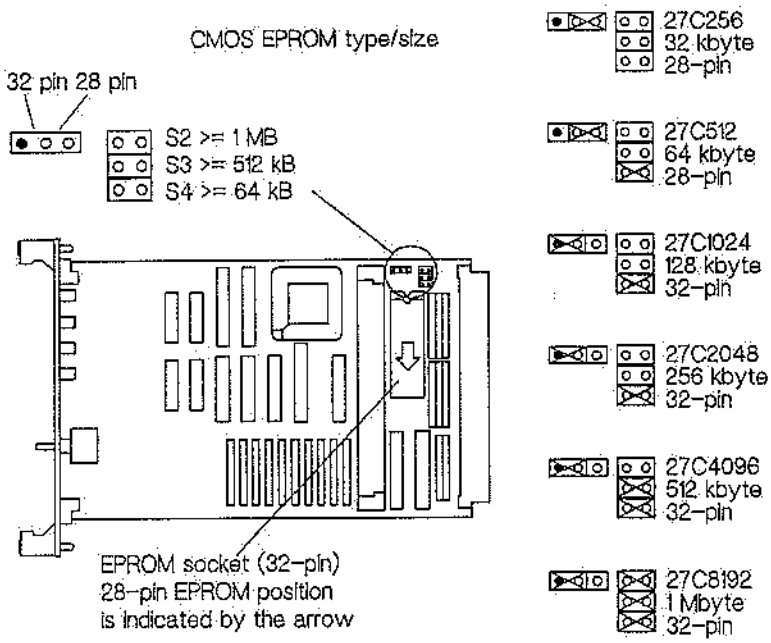
RAM memory	1 Mbyte D-RAM or 4 Mbyte D-RAM. 1 wait state. Cache bursts with 1 wait state per burst.
Internal bus	32-bit data bus.
Parity logic	One parity bit per byte in D-RAM, both for processor board memory and expansion memory. Halts the system at parity error.
EPROM size	Socket for 32kbyte - 1 Mbyte EPROM.
EPROM type	27C256 - 27C8192 ByteWyde CMOS EPROM in 32- or 28-pin DIP packet. Max 200 ns access time.
Switch	Reset position and 2 program readable positions.
Indicators	A parity error LED and 3 program controlled LEDs.
FPU	Optional MC68882 or MC68881. See the corresponding description.
Host connection	For the CPU30 processor board or equivalent.
Expansion	Expansion connector with internal bus and control lines enables additional expansion modules to be mounted.
Backplane	DataBoard I/O channel for power connection only. Bus termination resistors are provided on the EXP30 for the I/O channel.
Power	+5V +5%/-2.5%, 1.5A
Environment	0 - 55 °C, 10-80% noncondensing humidity.
Size	Single-height Eurocard.



Configuration

ESD protection is required, e g a wrist band connected to the computer chassis.

See the User Documentation Page where the user can enter the actual configuration. Depending on the selected EPROM circuit, set the appropriate jumpers according to the figure below.

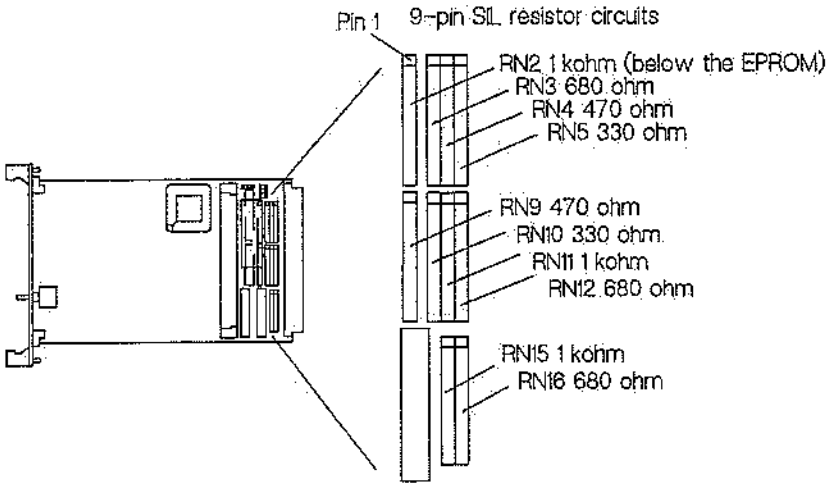


Optional FPU

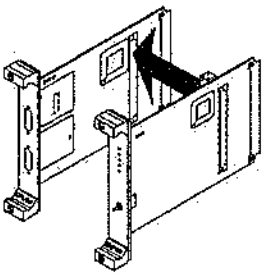
If used, the FPU is mounted according to the description for the FPU option.

DataBoard I/O channel terminations

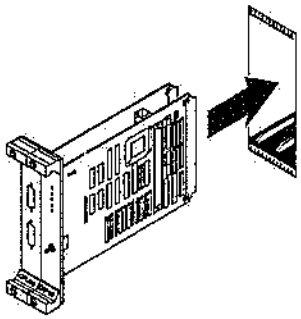
The following termination resistors shall be mounted unless corresponding terminations are used in the rack. Remove any terminations on the CPU module.



Installation



Connect the expansion board to the expansion connector on the processor module.

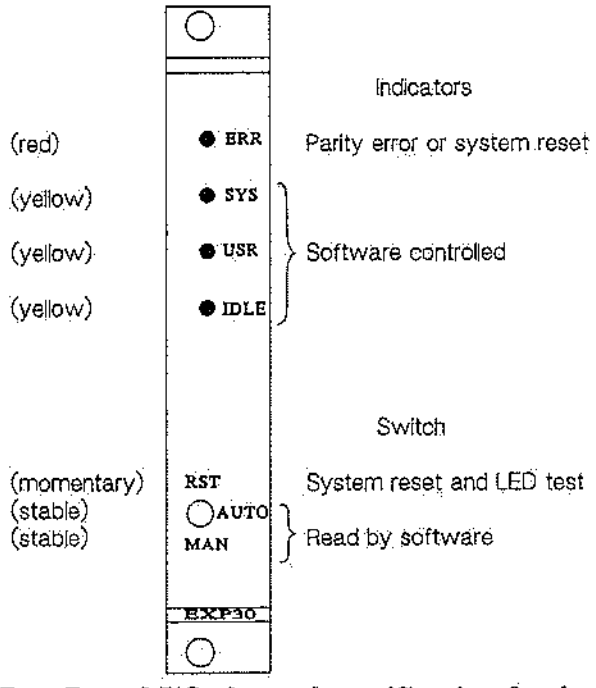


Turn off the power and insert the card stack in a DataBoard rack according to the rack description. Secure the modules to the rack with the four outer screws on the front.

Connectors, indicators and switches

The front panel contains four LED indicators and a manual switch. Three indicators are controlled and the switch read from the processor board through signals in the expansion connector.

System reset is generated either from the onboard switch or from an external source over the I/O channel (RST_IN*).

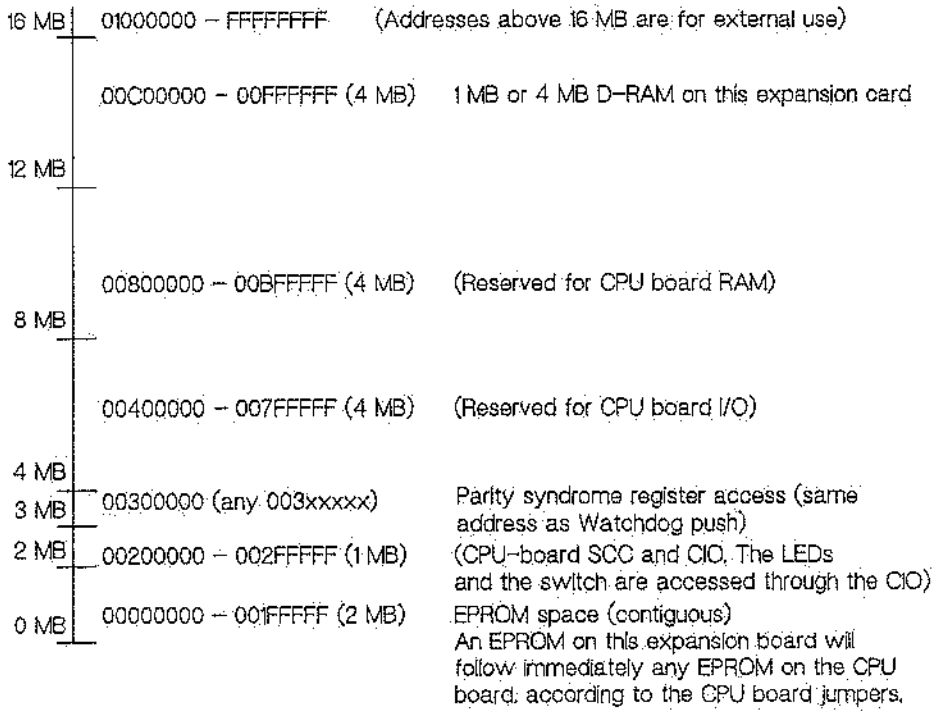


See the **DataBoard I/O channel specification** for the backplane connector description.

Programming

All resources are accessed within the same address space as the processor board (lower 16 Mbyte). The optional FPU is accessed through internal CPU instructions.

Physical address map:



Parity logic

One parity bit for each byte is generated at write cycles and checked at read cycles. The checked result is stored in the parity syndrome register. Once any parity syndrome bit is activated, it remains active until cleared by a watchdog write or a system reset. When a parity error is detected, further action depends on the expansion signal PB5 (from CIO port B, bit 5 on CPU30).

PB5 High	Default at power-on. A program must read the parity syndrome register to detect the error.
PB5 Low	The CPU is halted and the red ERR indicator is lit. Within 250 ms, a watchdog reset will reset the system and assert the DataBoard RST* signal, but the CPU will be held halted until a hardware system reset or power off/on.

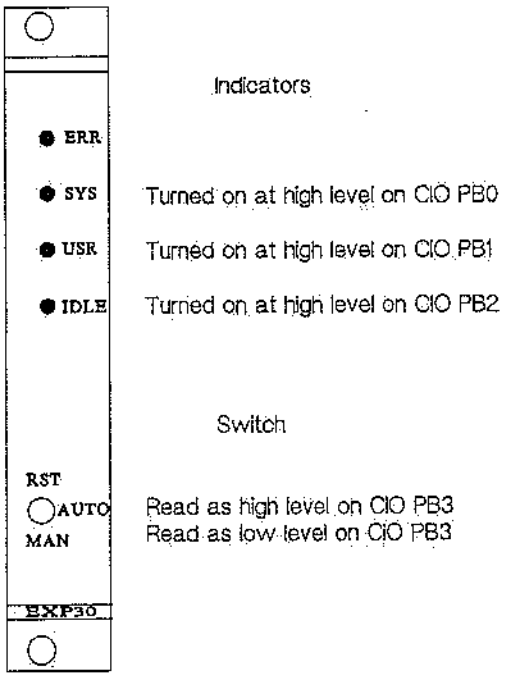
With a passive parity logic (PB5 high), the parity generation/check function can be verified. Reading the parity syndrome register provides the following.

Parity syndrome	Description
Bit 0 Low	Parity error in D31 - D24
Bit 1 Low	Parity error in D31 - D24
Bit 2 Low	Parity error in D31 - D24
Bit 3 Low	Parity error in D31 - D24
Bit 6 Low	Parity error in lower memory bank 8-12 Mbyte (otherwise on expansion memory bank 12-16 Mbyte)

For testing the parity memory circuits, parity errors can be created by using MOVES instructions with zero function code (FC=0), which will store inverted parity bits. A memory read will then result in an error in the parity syndrome register.

LEDs and switches
The three yellow LEDs are controlled by the CIO port B, bit 0 - 2, on the processor board through the expansion connector lines PB0 - PB3.

The switch positions (AUTO or MAN) can be read by the program through the CIO port B, bit 3, which is PB3 on the expansion connector.



Power-up/reset sequence
At power-on/reset all front panel indicators are turned on. The error indicator is immediately turned off unless a parity error occurs, but the other indicators are turned off by the program.

A parity error (ERR) is cleared only at power-on or a hard reset from the switch or from the DataBoard I/O channel. It is not cleared at a watchdog reset on the CPU board.

References

DataBoard I/O channel specification.

CPU30, MC68030 Processor board, module description.

FPU, Floating point unit for EXP30, module description.

Version information

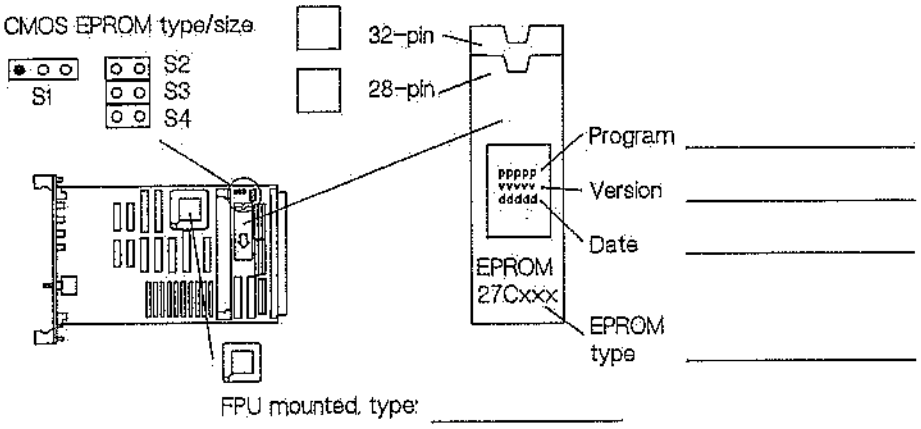
Document:
A First version

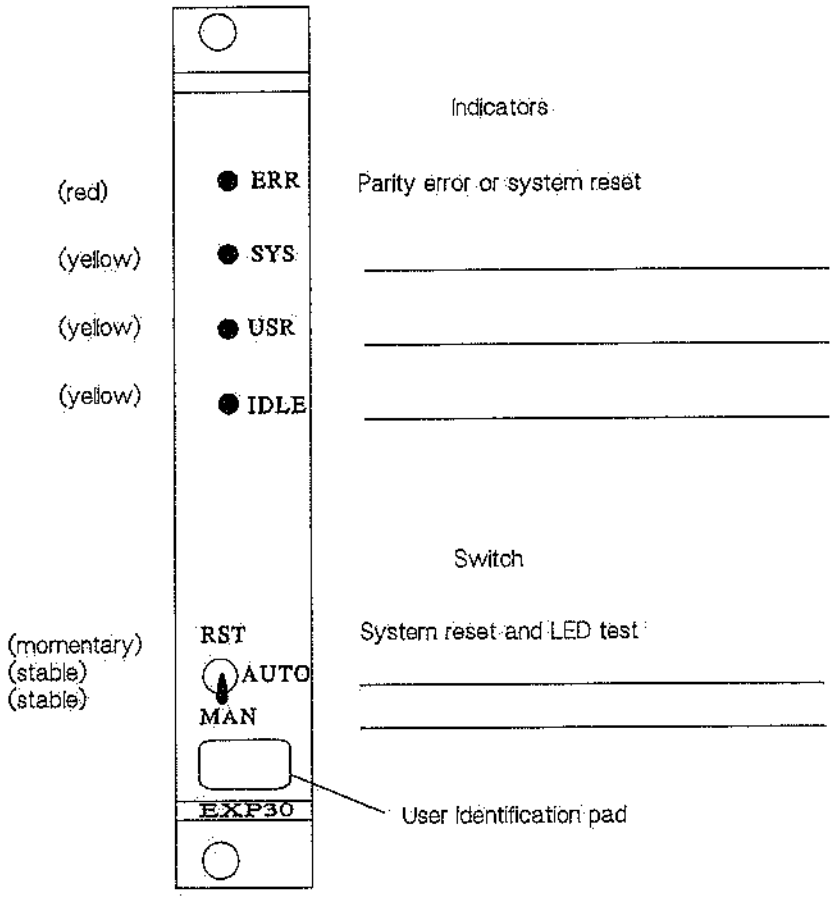
User documentation page

Project: _____ Date: _____

_____

D-RAM memory size: _____ Mbyte





EXP30, Expansion board for CPU30 module description

002-1031-xx
Version A

Please give us your opinion on our documentation. Either tell us on this page or make a copy of the page concerned. Staple it to this page and mail it to us.

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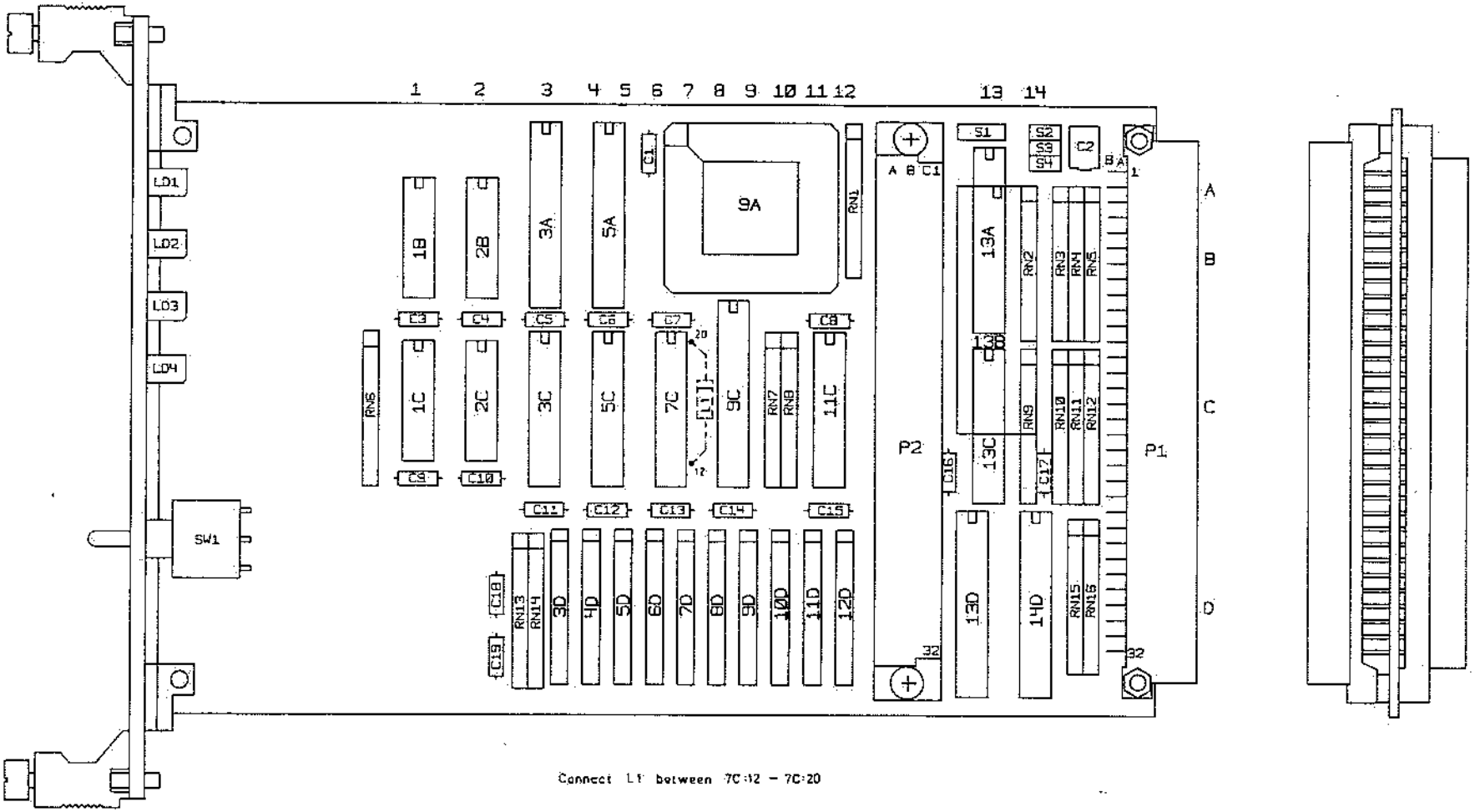
DIAB DATA



Connect L1 between 7C:12 – 7C:20

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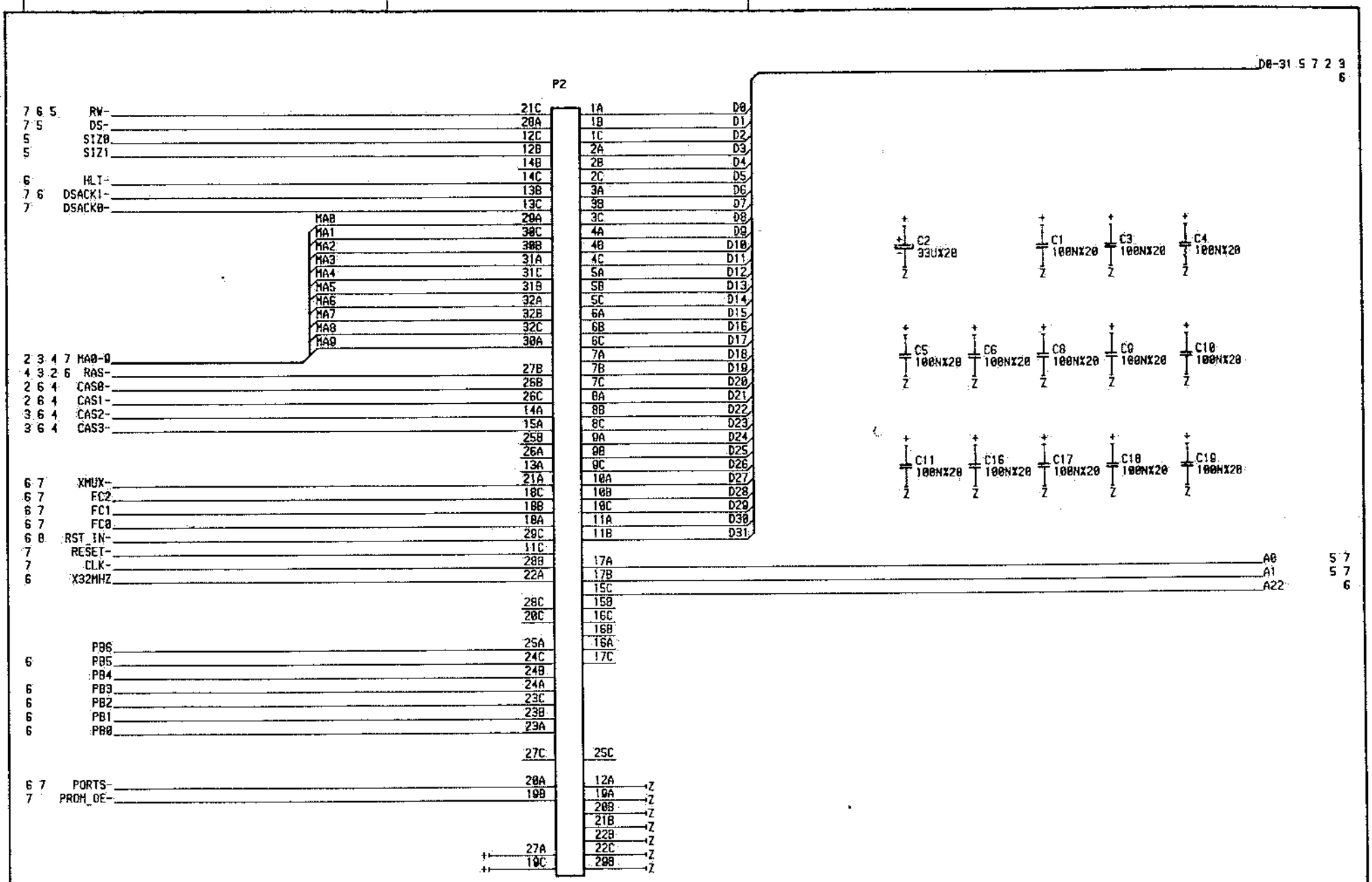
			901218	DATE	DRAWN	KP 900211			82-1031-10



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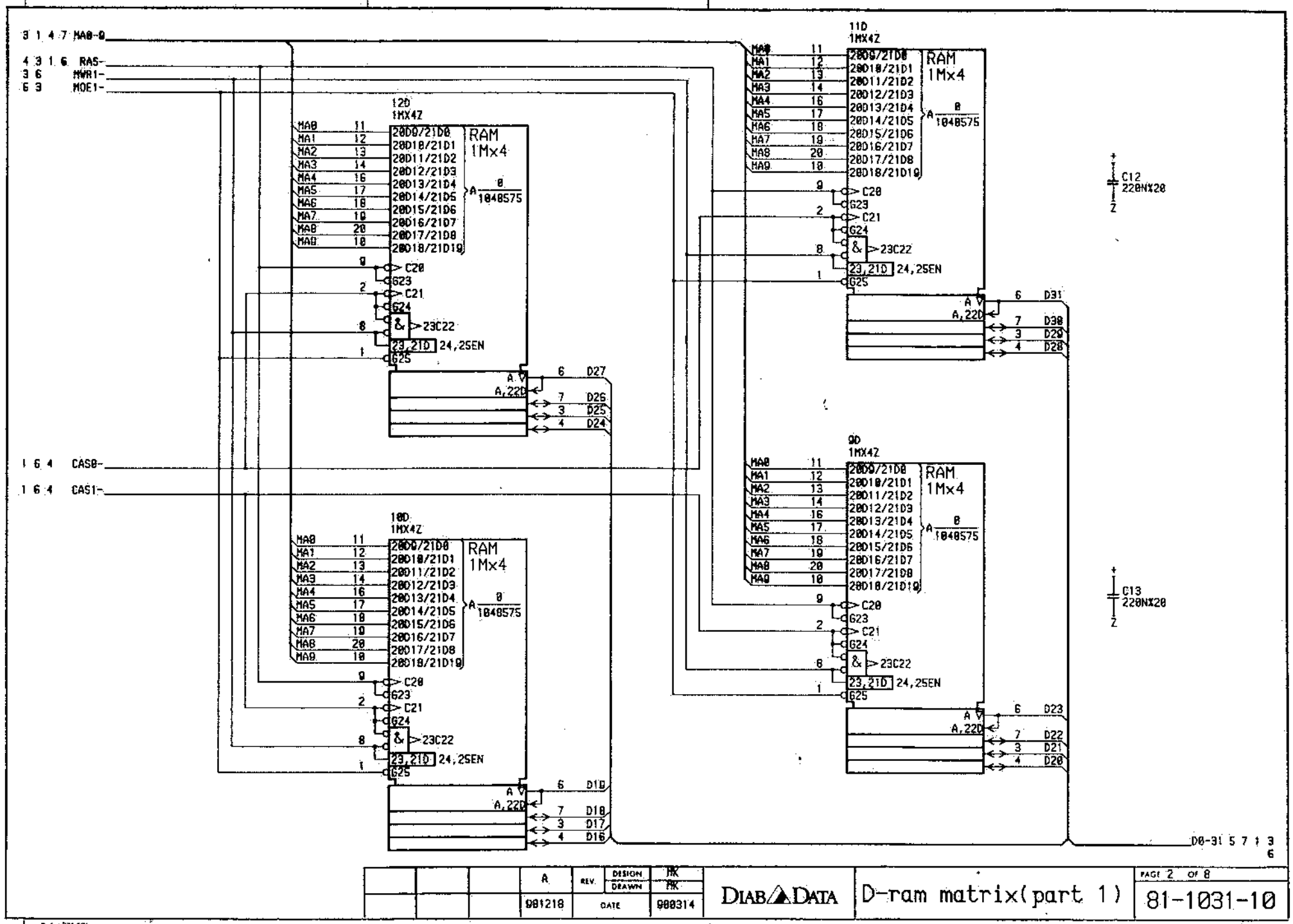
			981218	DATE		980314	

DIAB DATA

Expansion connector

PAGE 1 OF 8

81-1031-10



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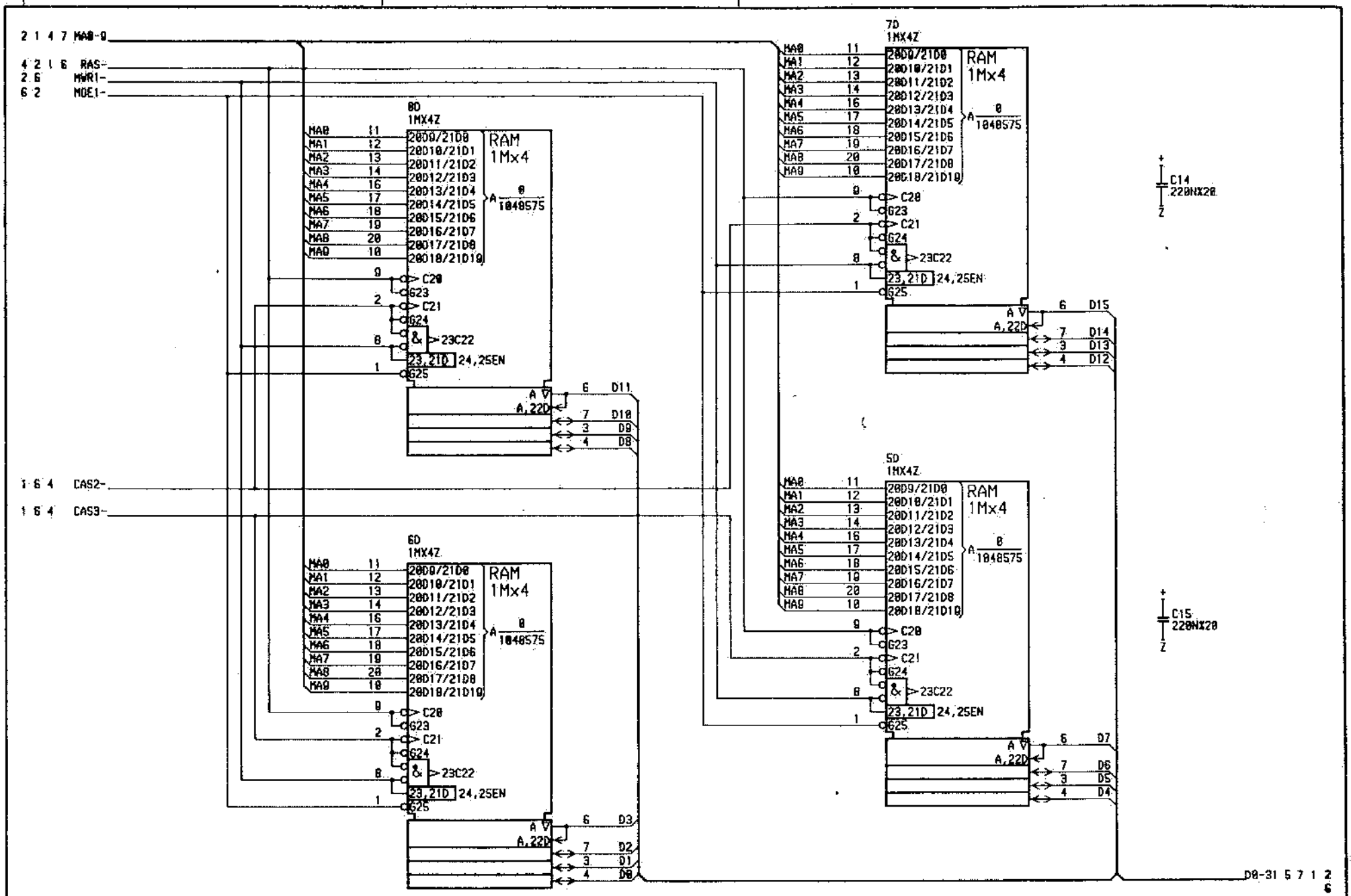
			981218	DATE	DRAWN	MK 980314		81-1031-10

PAGE 2 OF 8



			A	REV.	DESIGN	MK	
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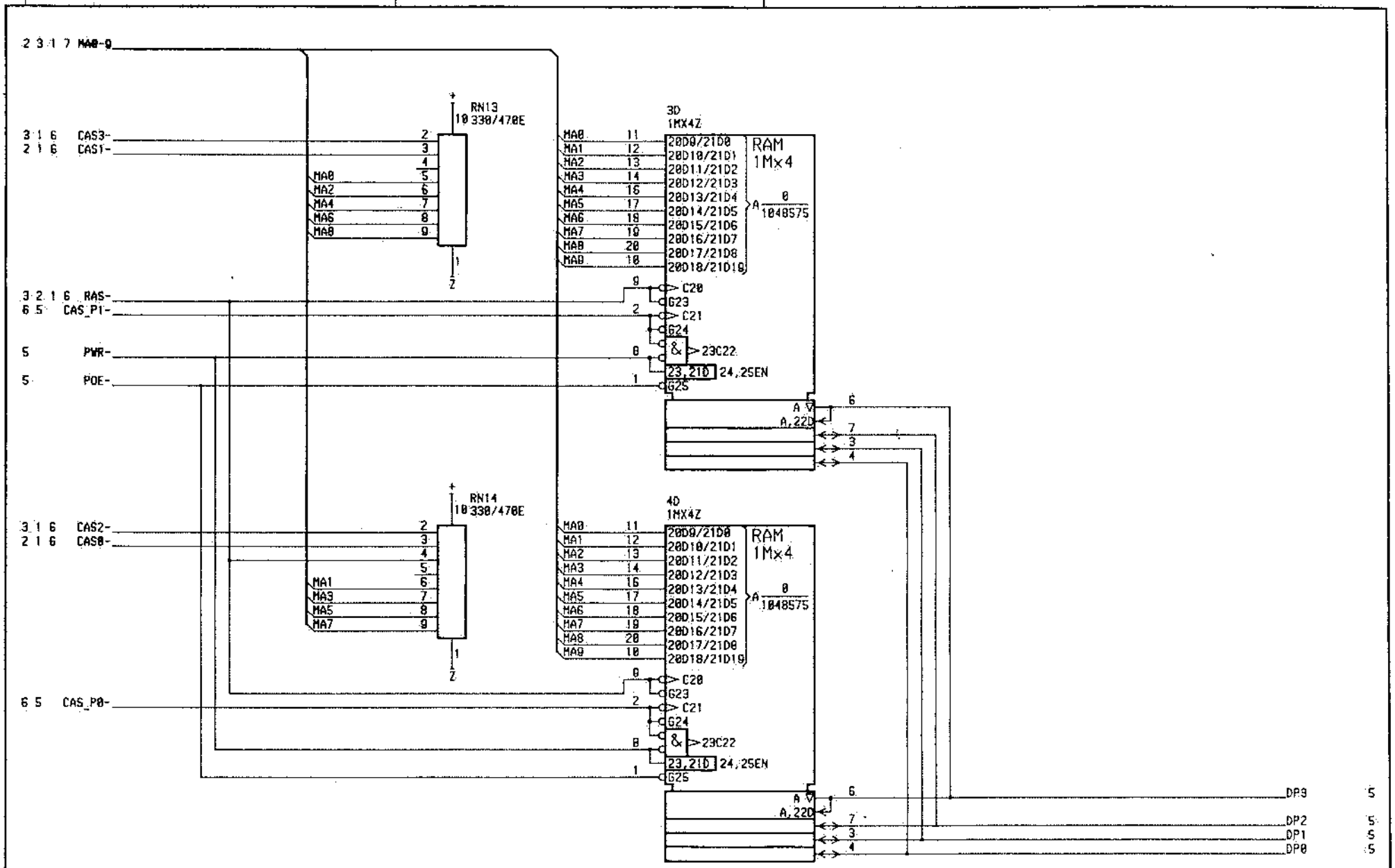
			881218	DATE		890314	

DIAB DATA

D-ram matrix(part 2)

PAGE 3 OF 8

81-1031-10



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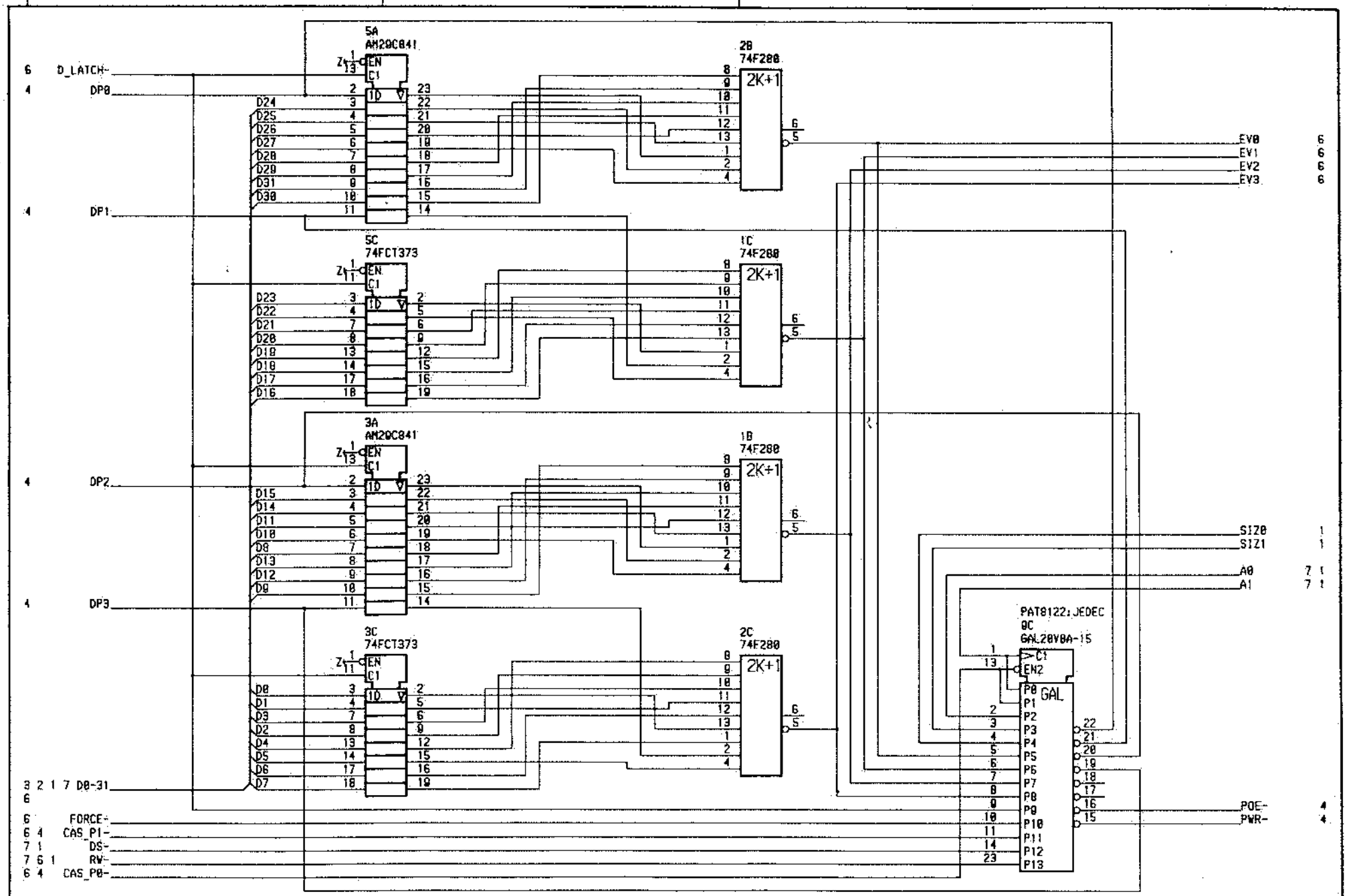
			881218	DATE	DRAWN	MK 880314

DIAB DATA

D-ram matrix(parity)

PAGE 4 OF 8

81-1031-10



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			081218	DATE	DRAWN	HK			81-1031-10
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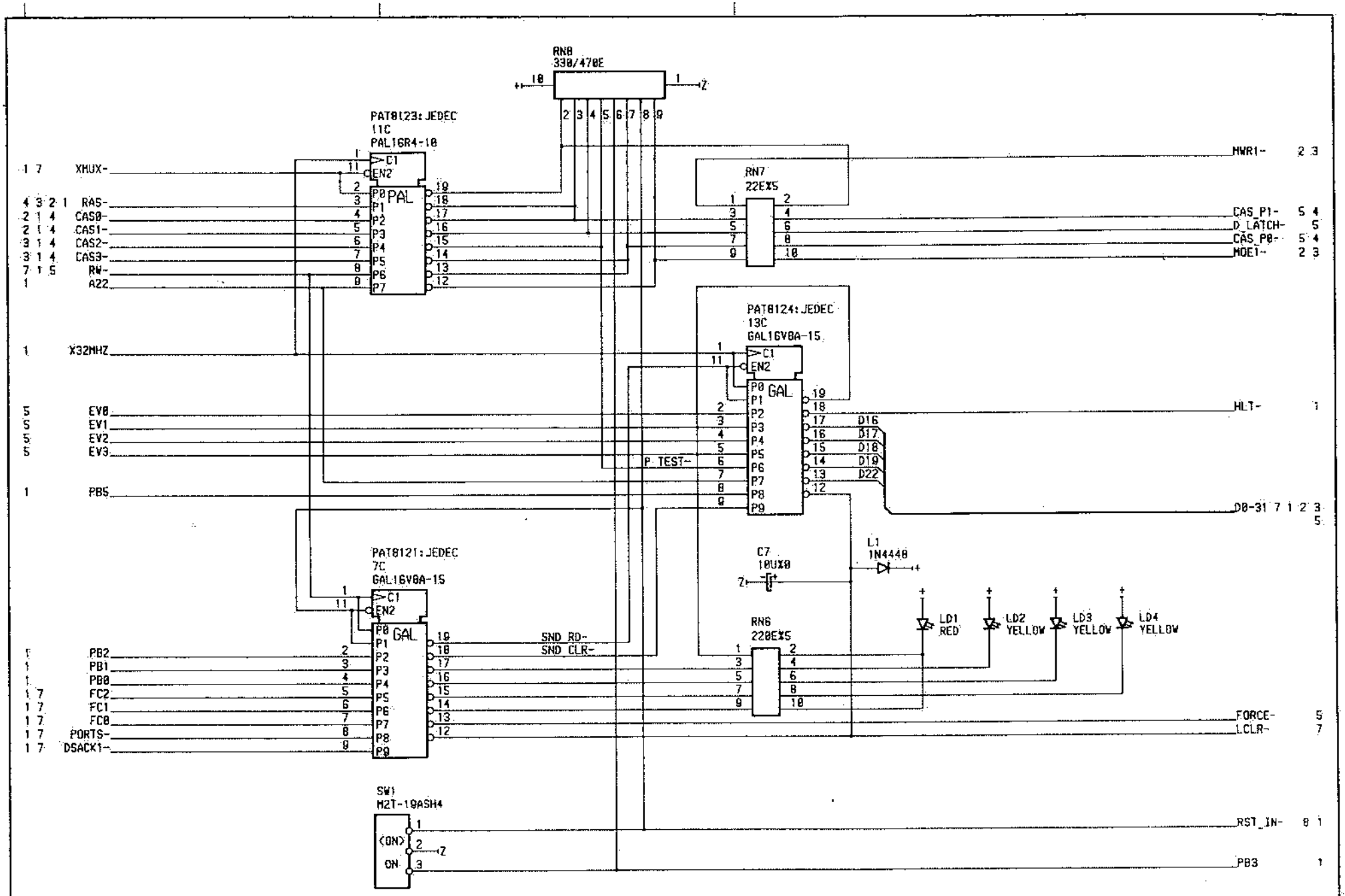

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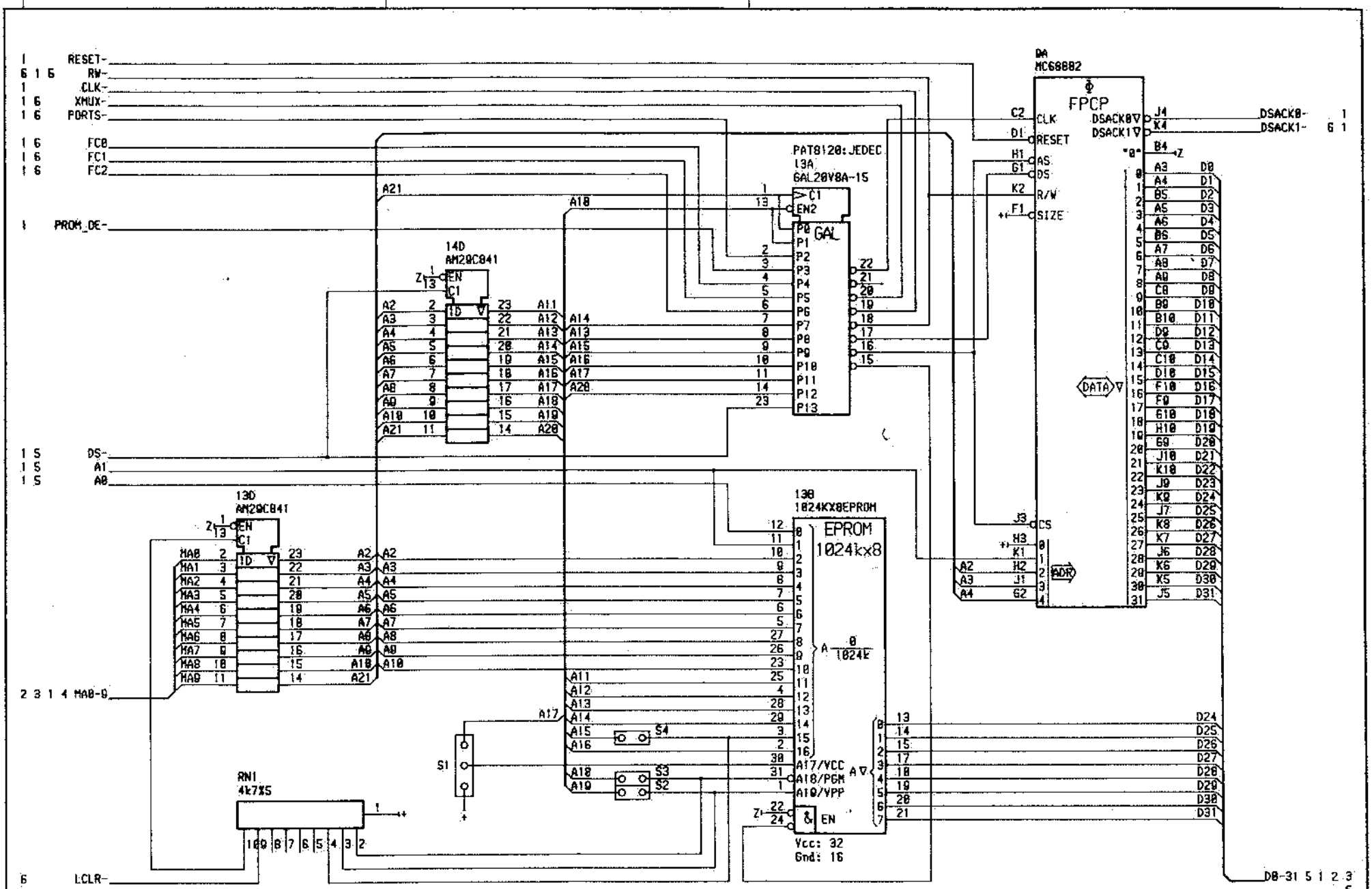
					980314			PAGE 6 OF 8



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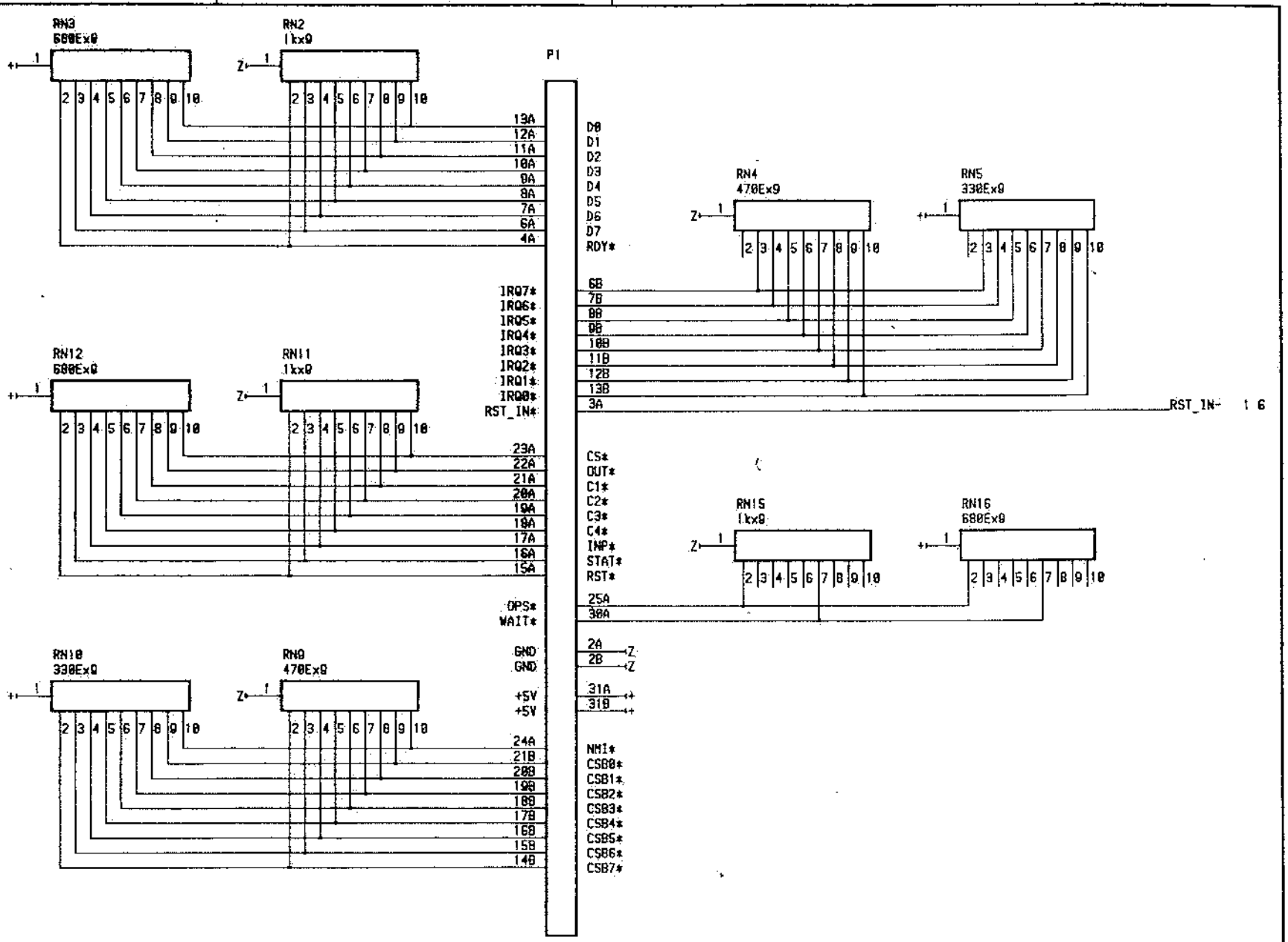
DIAB DATA

FPCP and EPROM

PAGE 7 OF 8

81-1031-10



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PAGE 8 OF 8